# GaN Transistors for Efficient Power Conversion

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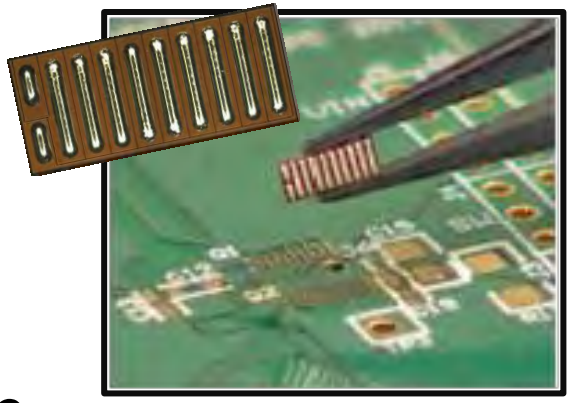
and David Reusch
Efficient Power Conversion



# Agenda



- How GaN works and the state-of-the-art
- Design Basics
- Design Examples
- What is in the future?

# How GaN Works and the State-of-the-Art

# Power Switch Wish List



- Lower On-Resistance
- Faster
- Less Capacitance
- Smaller
- Lower Cost

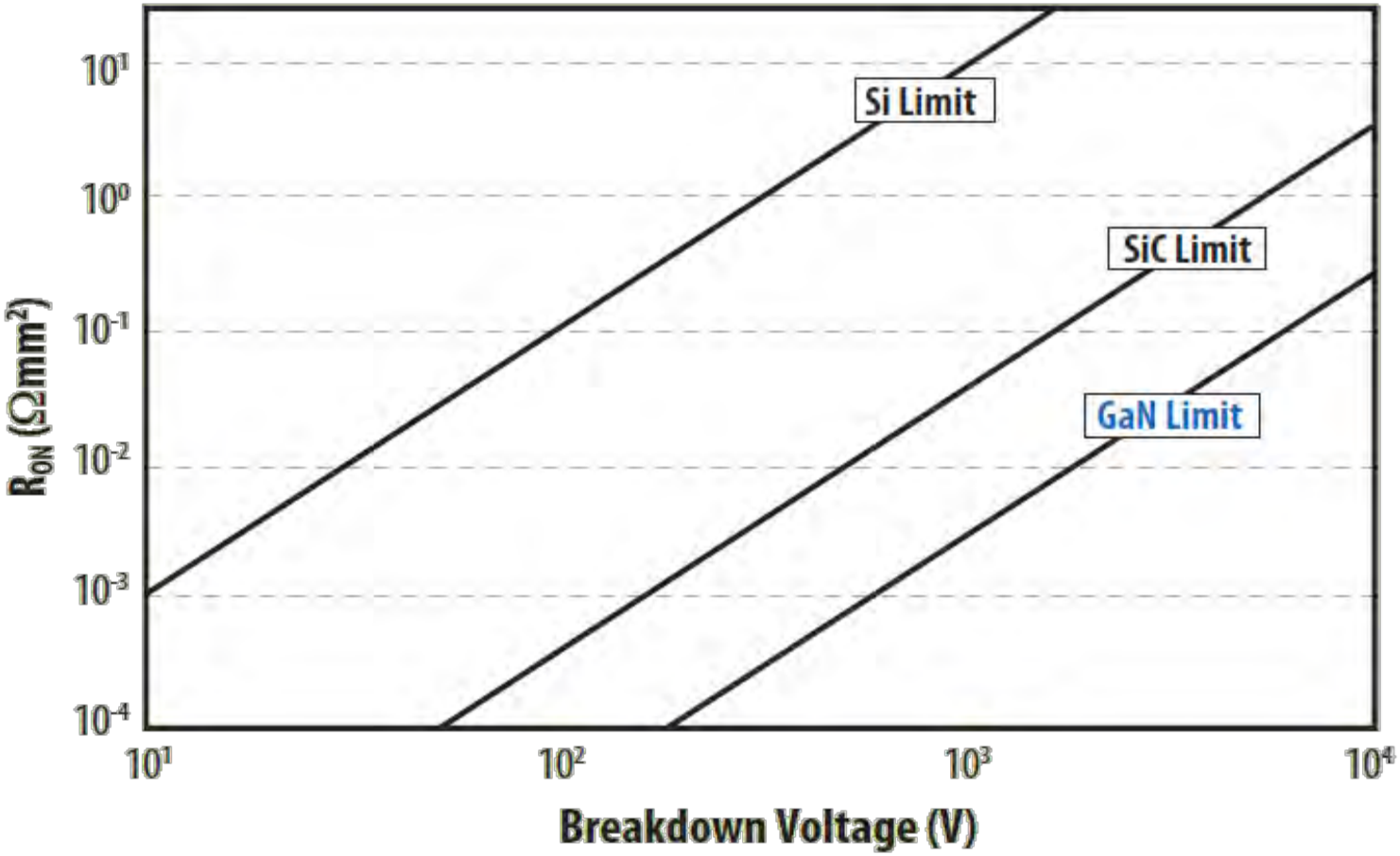
# Material Comparison



| Parameter | | GaN | Silicon | SiC |
|---|---|---|---|---|
| Band Gap $E_g$ | eV | 3.2 | 1.12 | 3.4 |
| Breakdown Field $E_{BV}$ | MV/cm | 3.3 | 0.3 | 3.5 |
| Electron Mobility $\mu_n$ | $cm^2/V \cdot s$ | 2000 | 1500 | 650 |

# State of the Art

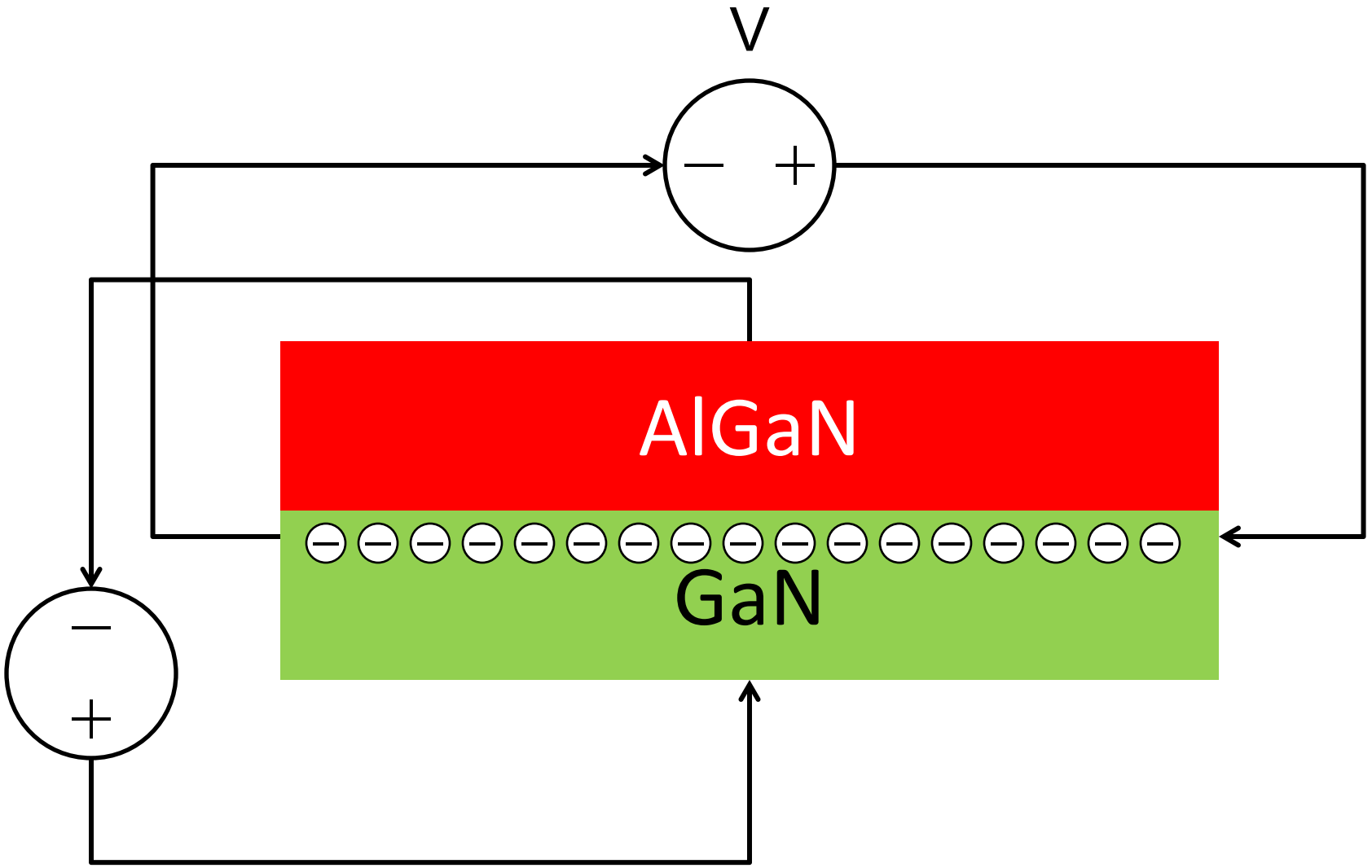




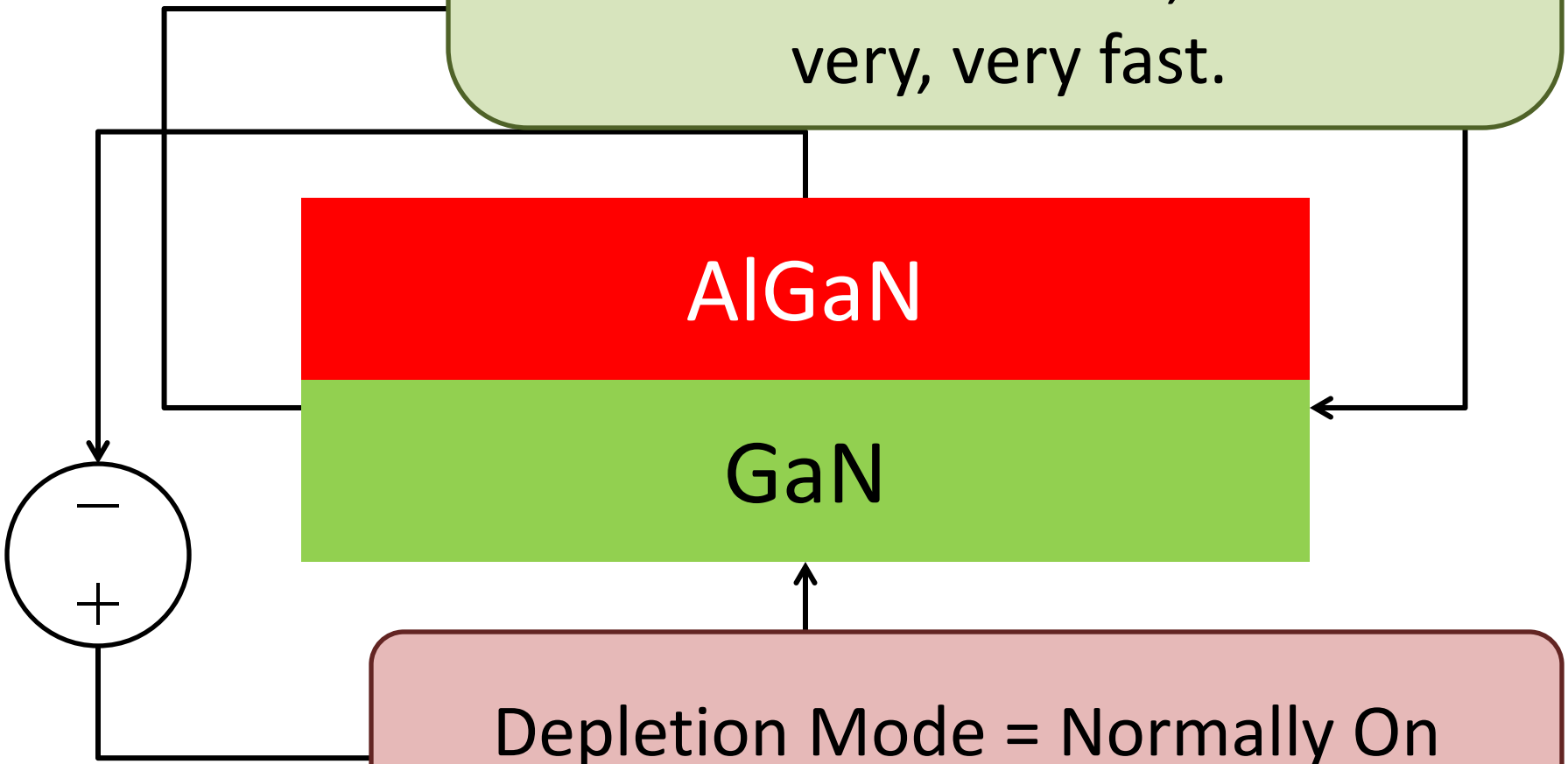

Theoretical on-resistance vs. blocking voltage capability for silicon, silicon carbide, and gallium nitride.

# GaN Switch

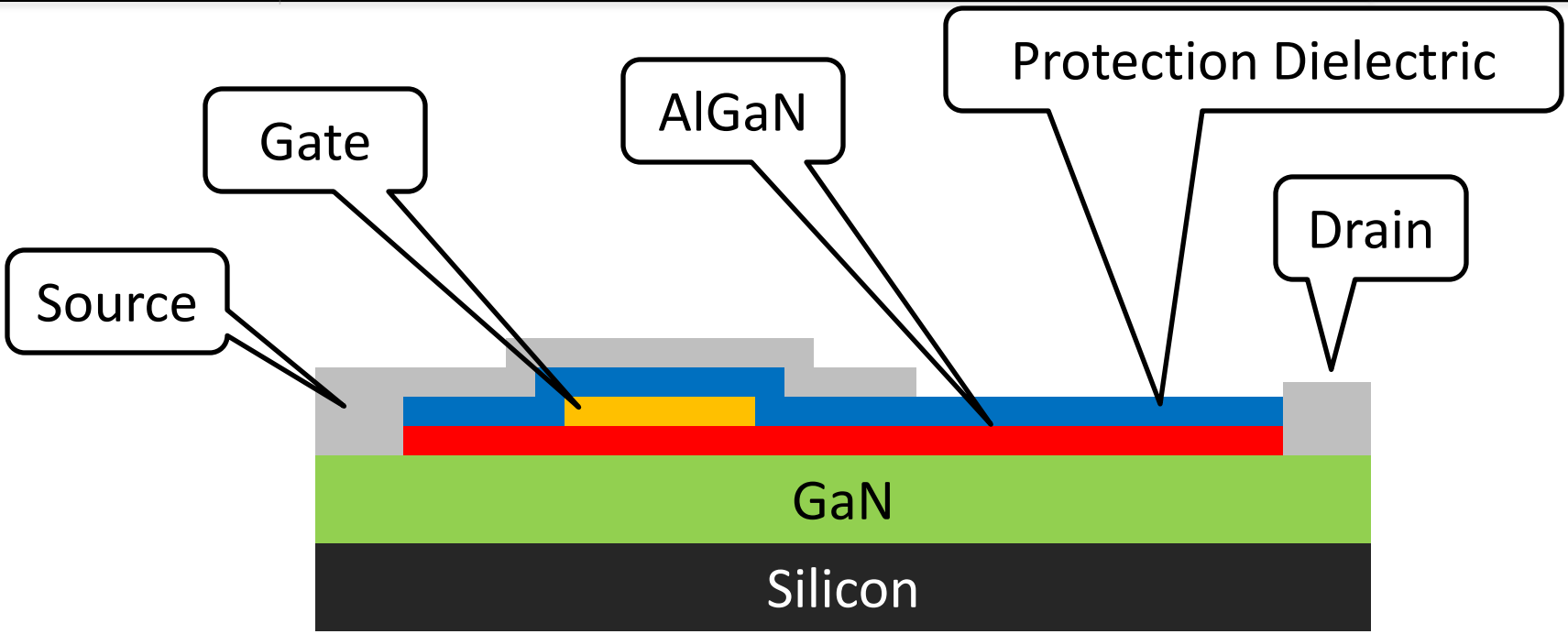




Now we have a switch
That has high voltage blocking capability,
low on resistance, and is
very, very fast.



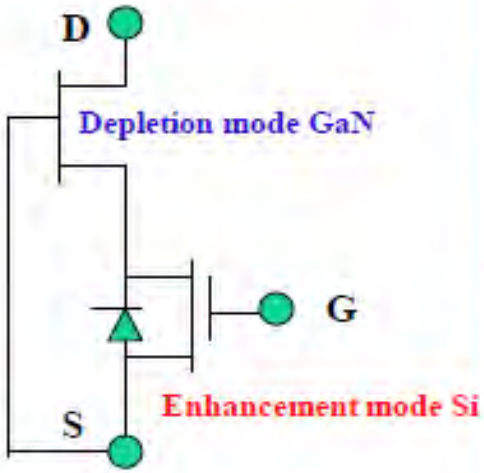
# Device Construction Concept



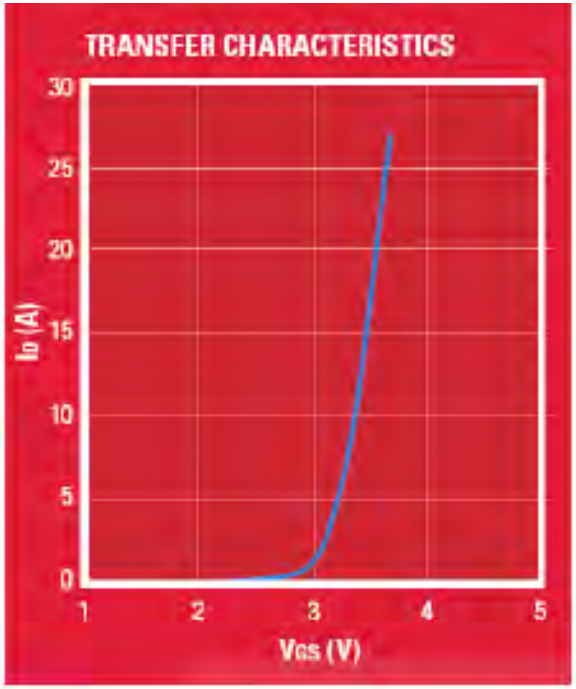
# What about "Normally Off" devices?

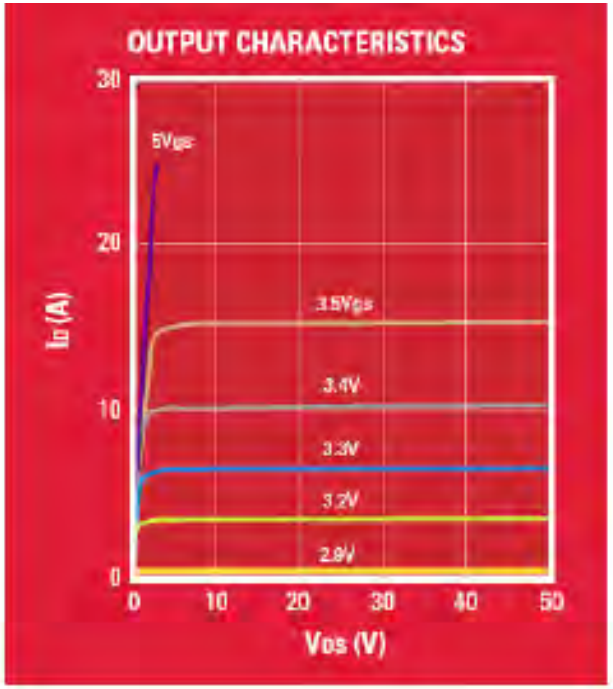
# Cascode GaN Device






Cascoded Switch




## Highlights:

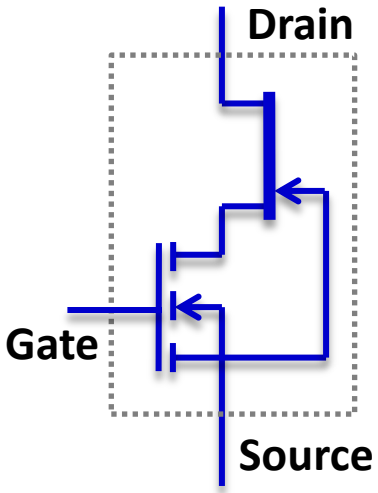
- Normally Off operation
- Gate drive compatible with existing Silicon solutions: +/-10V, +/- 15V , etc.
- Vgs(th) can be tailored with Si FET: high enough to avoid C*dV/dt induced turn on
- Anti-parallel diode function included: lower reverse recovery losses than Si switches

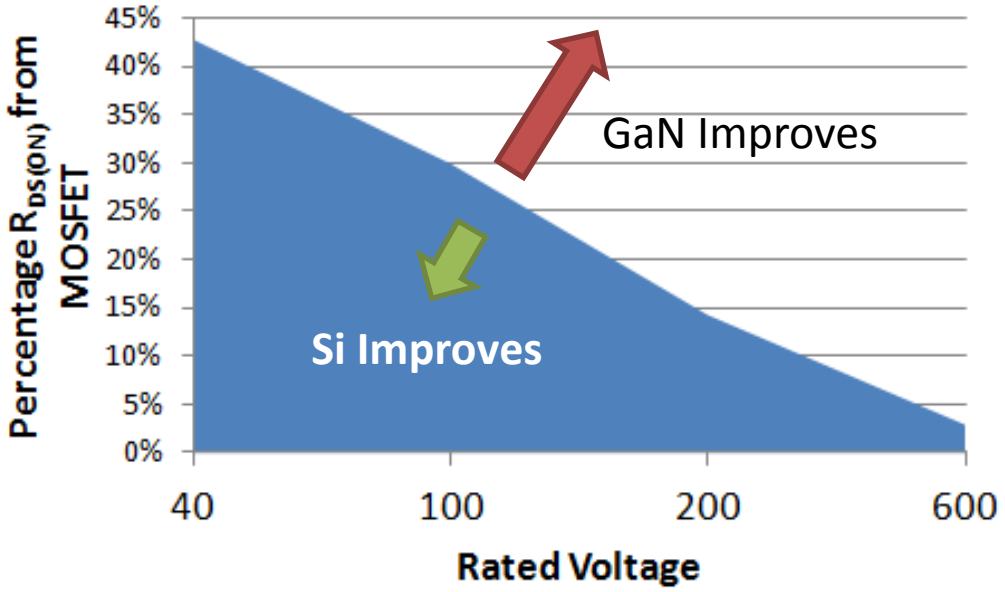
**Reference: "The Status of GaN Power Device Development at International Rectifier," PCIM 2012**

# Cascode Penalty



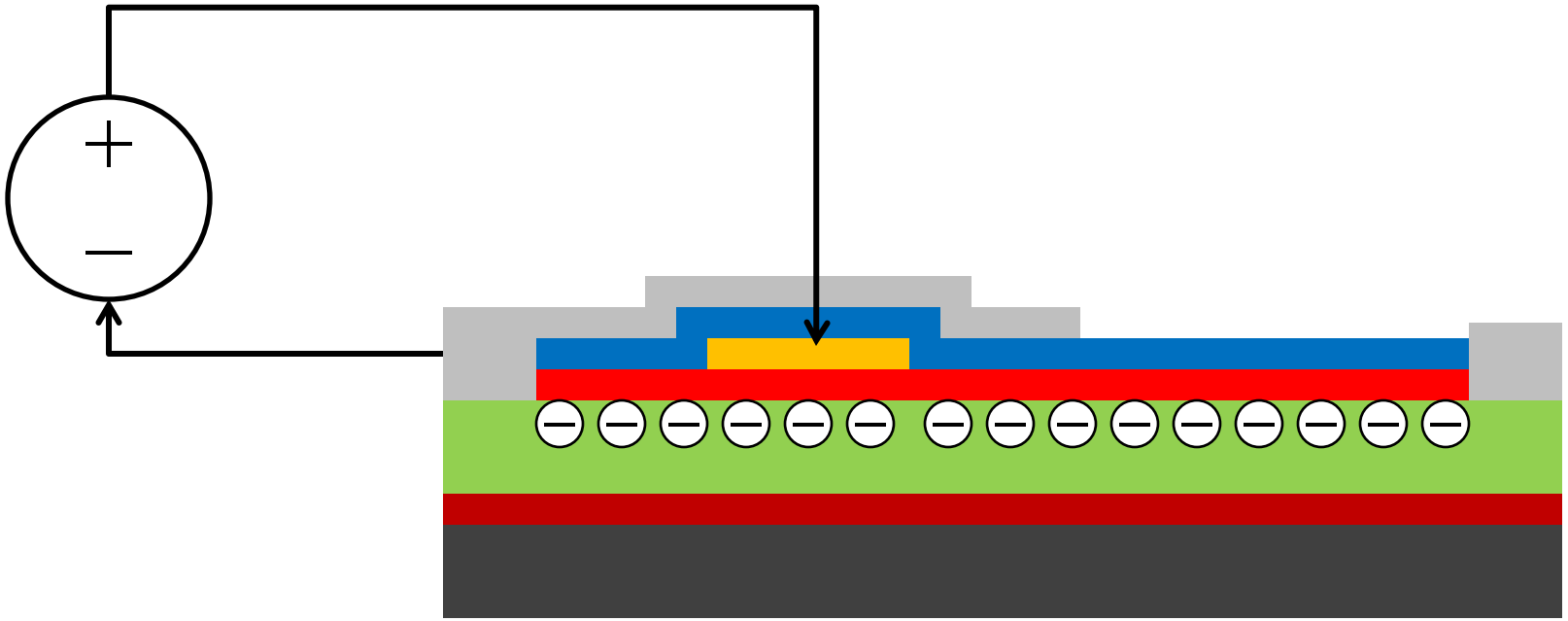
Cascode devices combine a depletion mode GaN transistor with a low voltage enhancement mode MOSFET



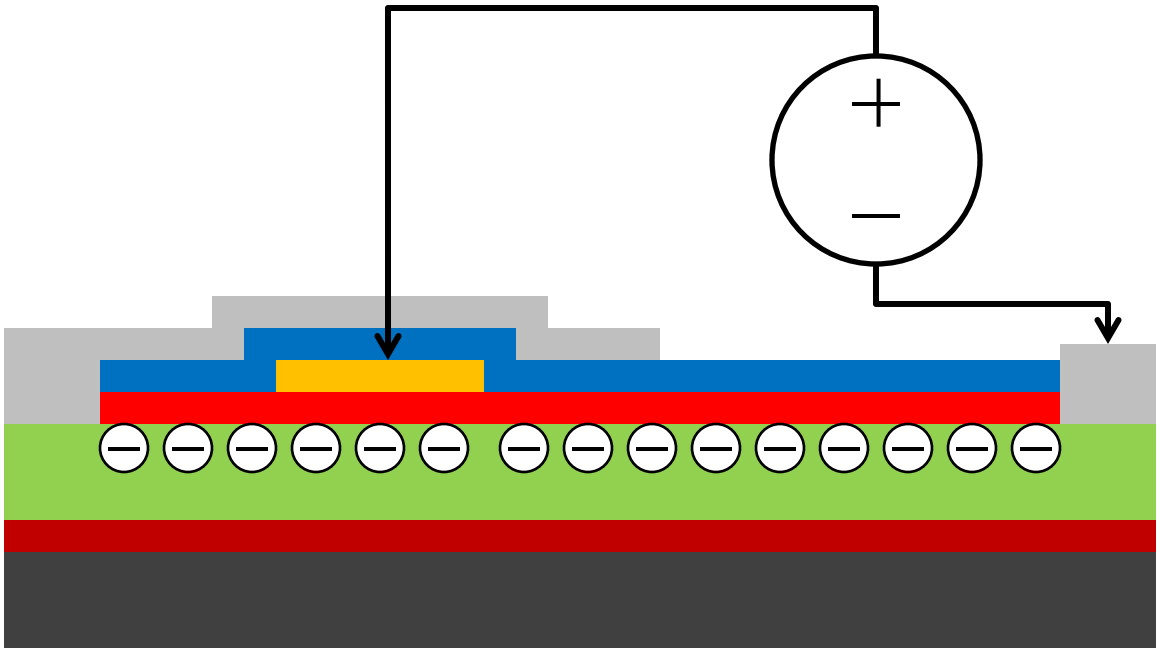
# Enhancement Mode





A positive voltage from Gate-To-Source establishes an electron gas under the gate

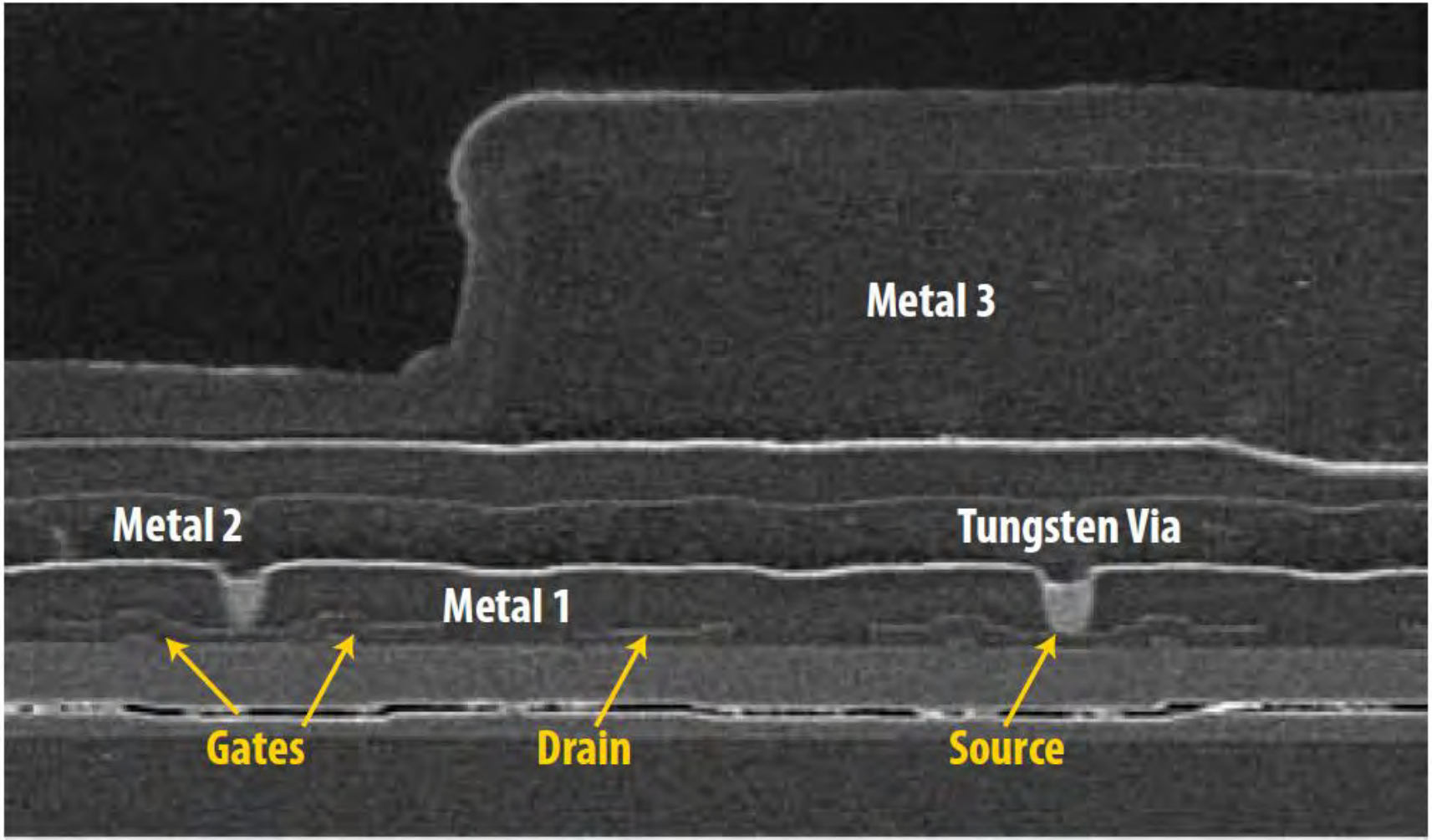
# Body Diode?



A positive voltage from Gate-To-Drain
also establishes an electron gas under the gate

# Cross Section of an eGaN® FET

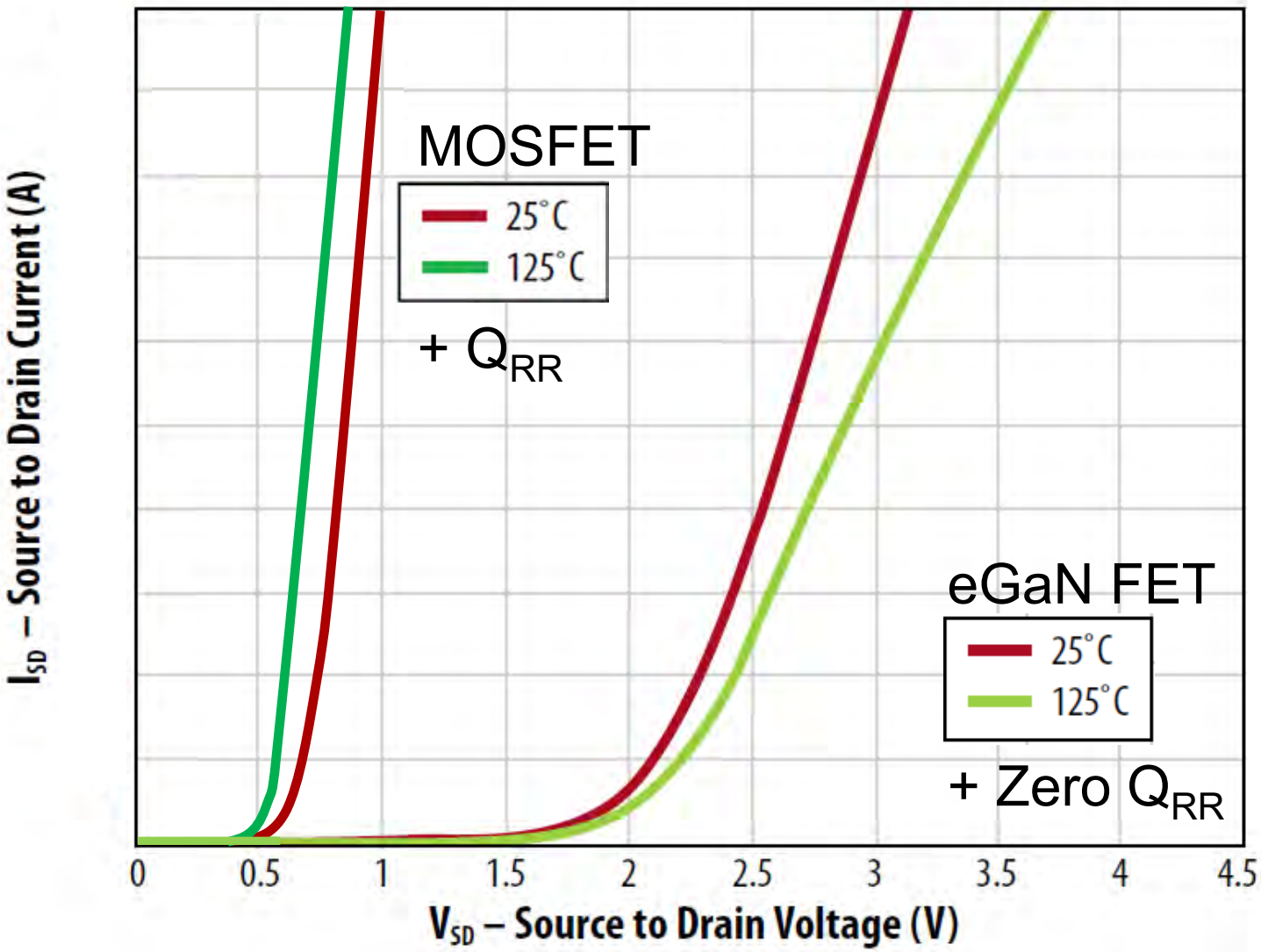




# Electrical Characteristics

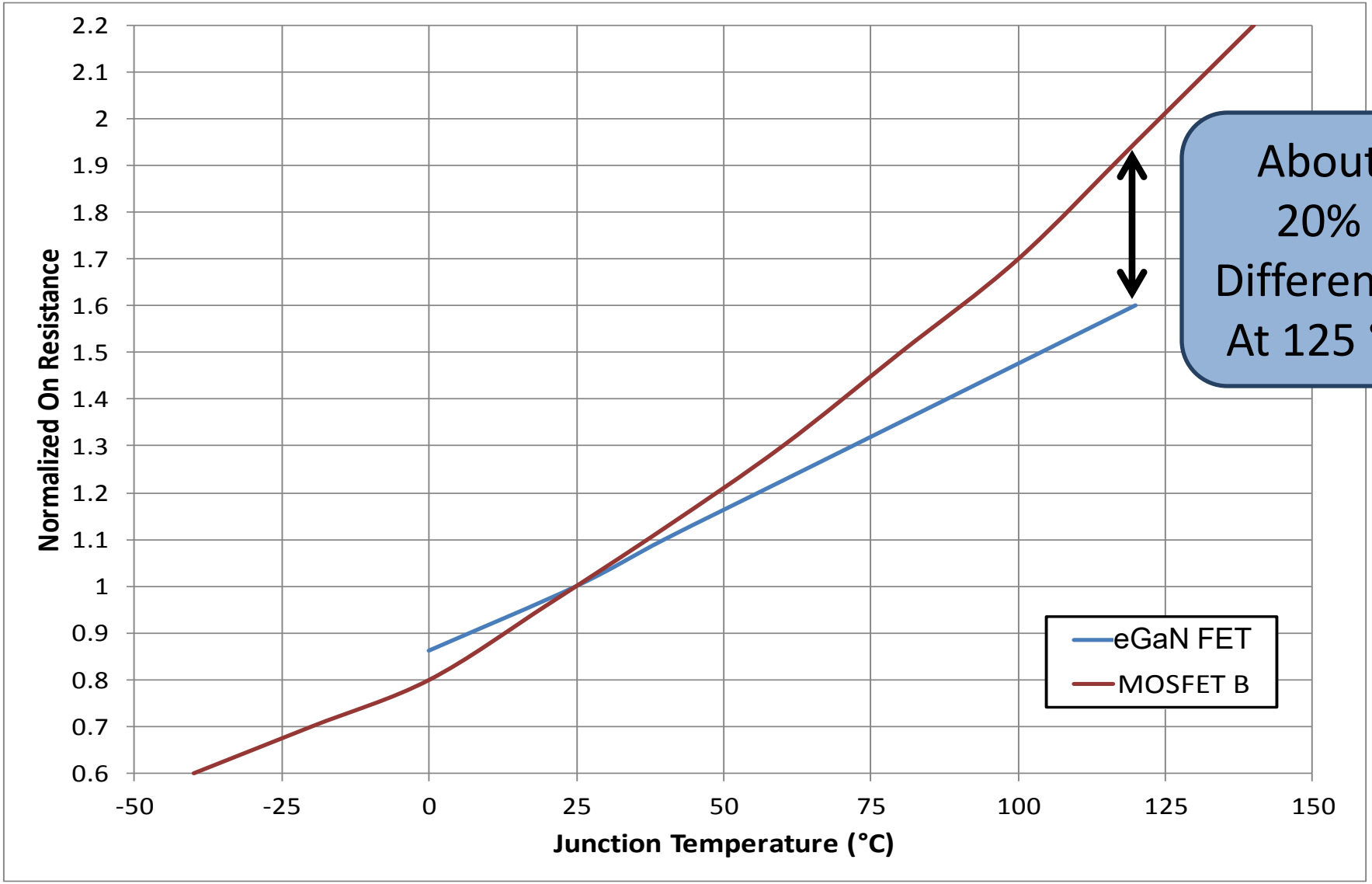
# eGaN FET Reverse Conduction



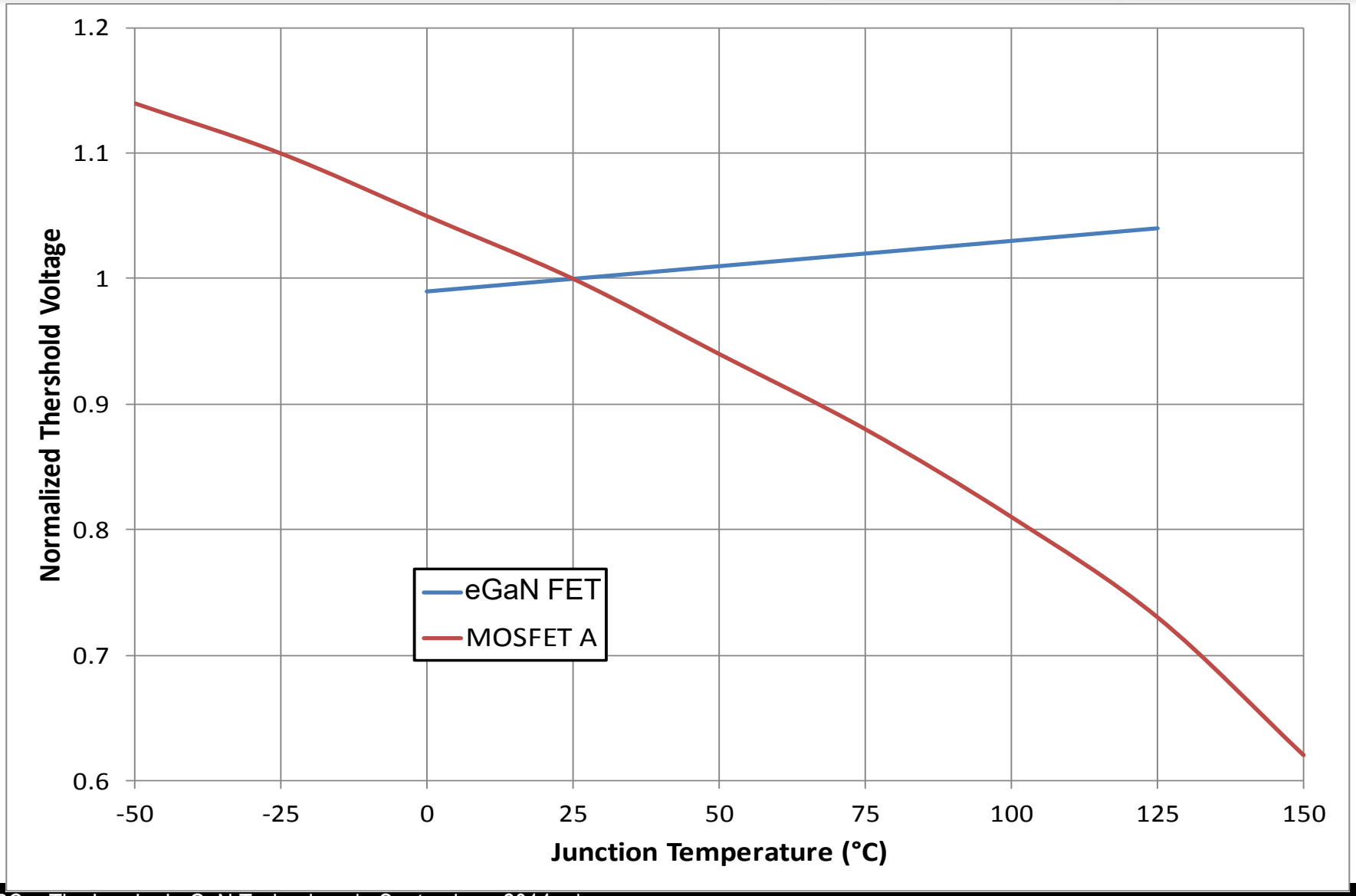


# On Resistance vs. Temperature





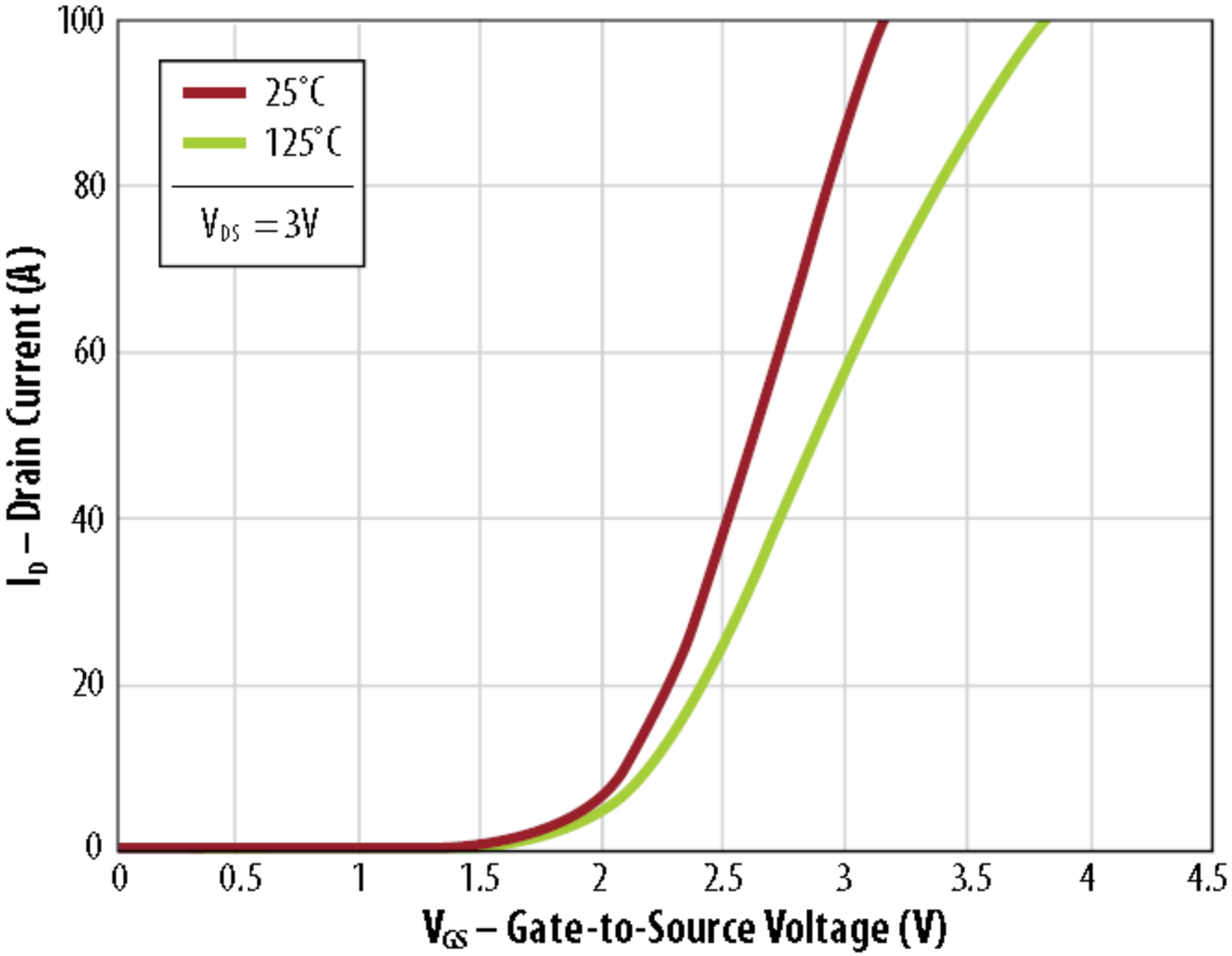
# Threshold vs. Temperature



# eGaN FET Transfer Characteristics



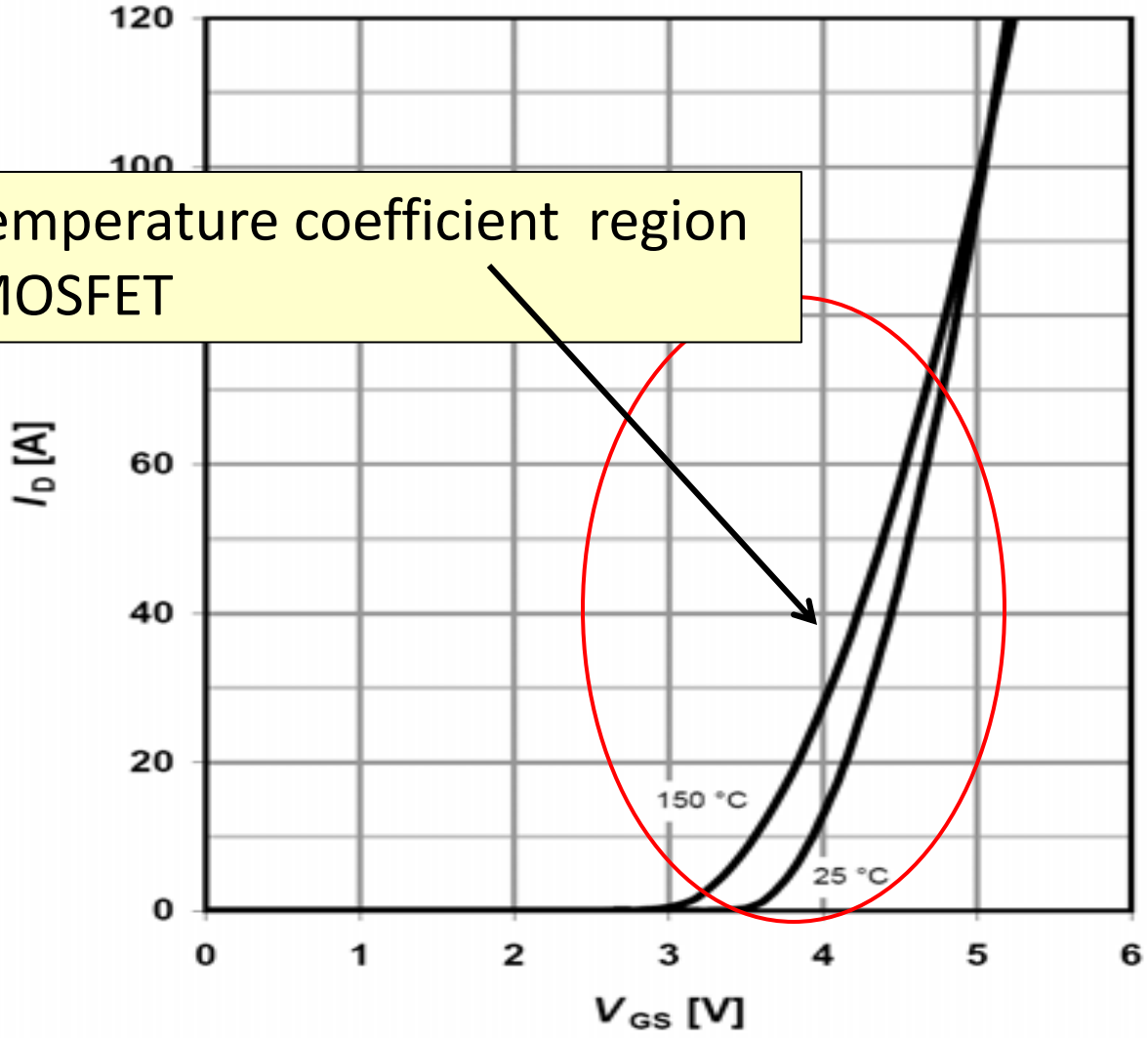
## EPC2001



# MOSFET Transfer Characteristics



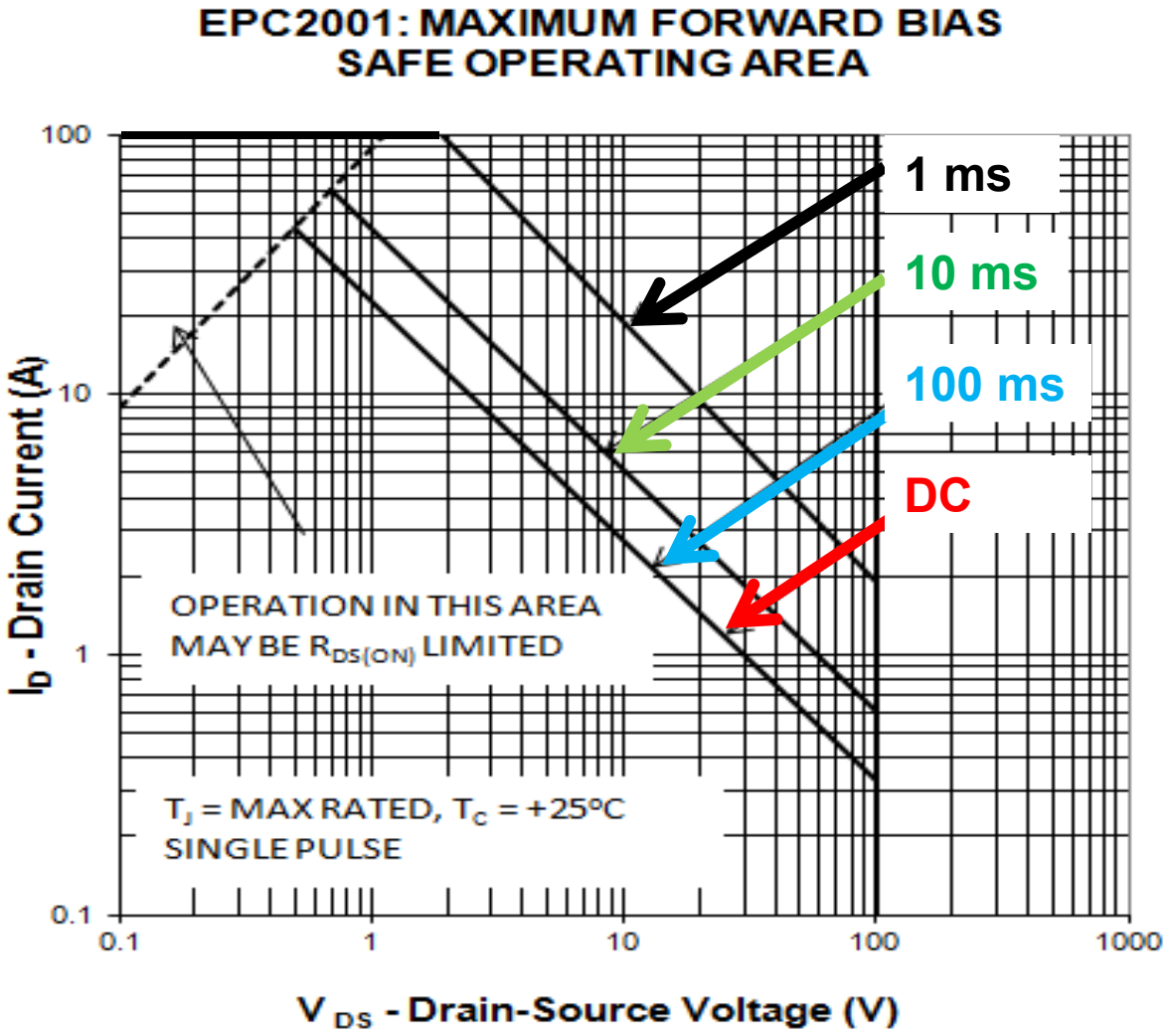
Negative temperature coefficient region of silicon MOSFET




Source: www.infineon.com

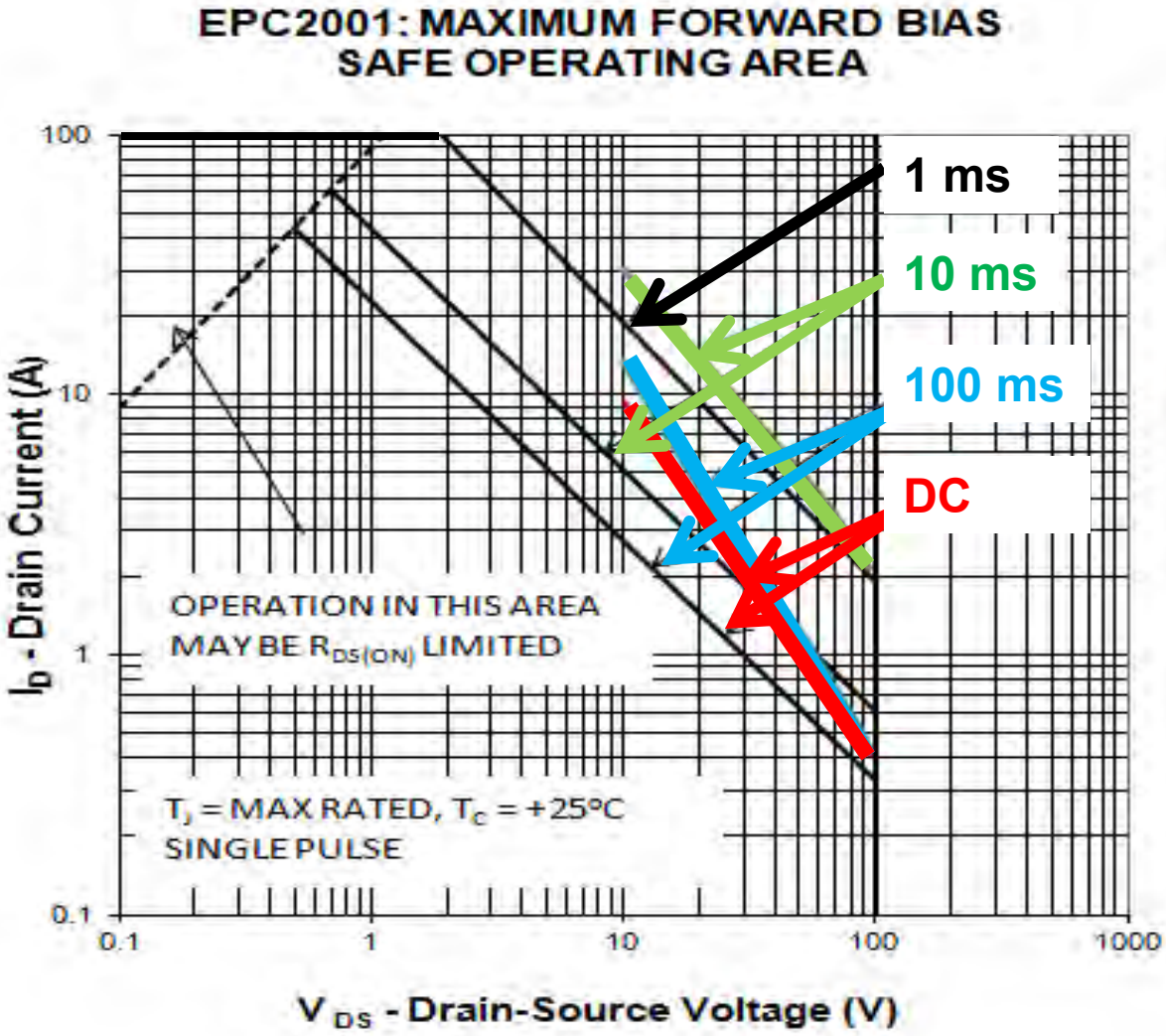
# eGaN FET Safe Operating Area





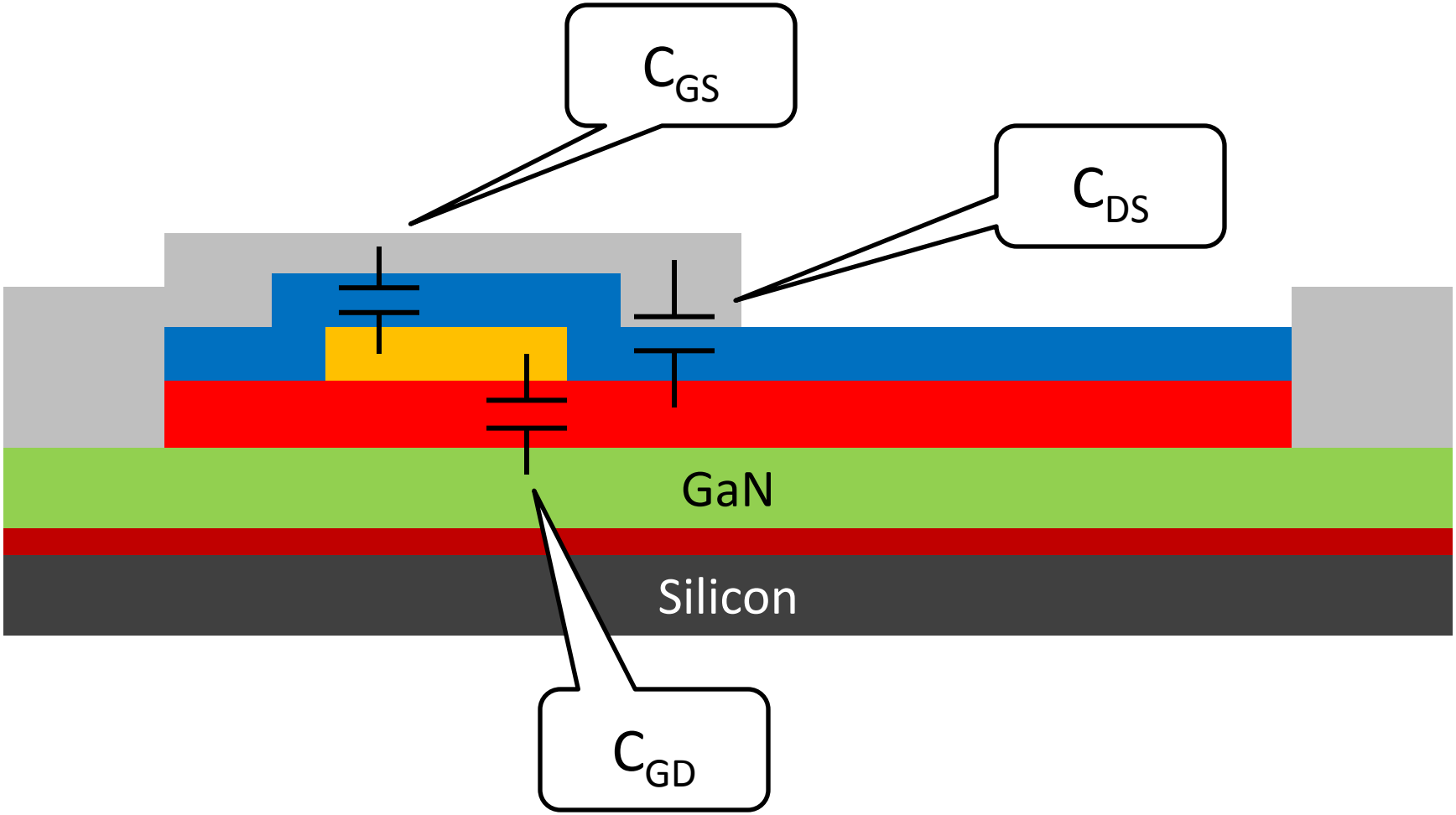
# eGaN FET Safe Operating Area





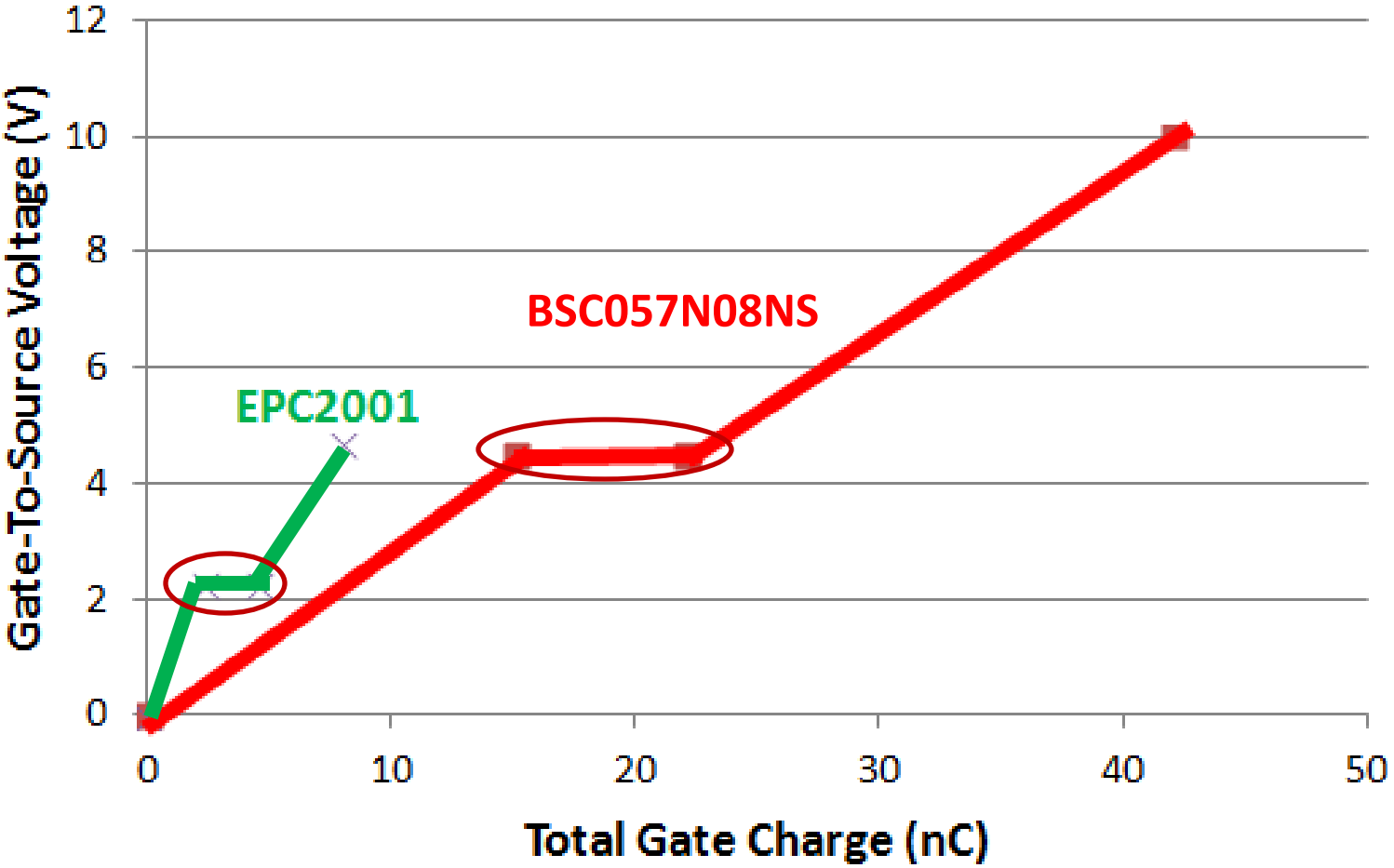
# eGaN FET Capacitances





# Total Gate Charge



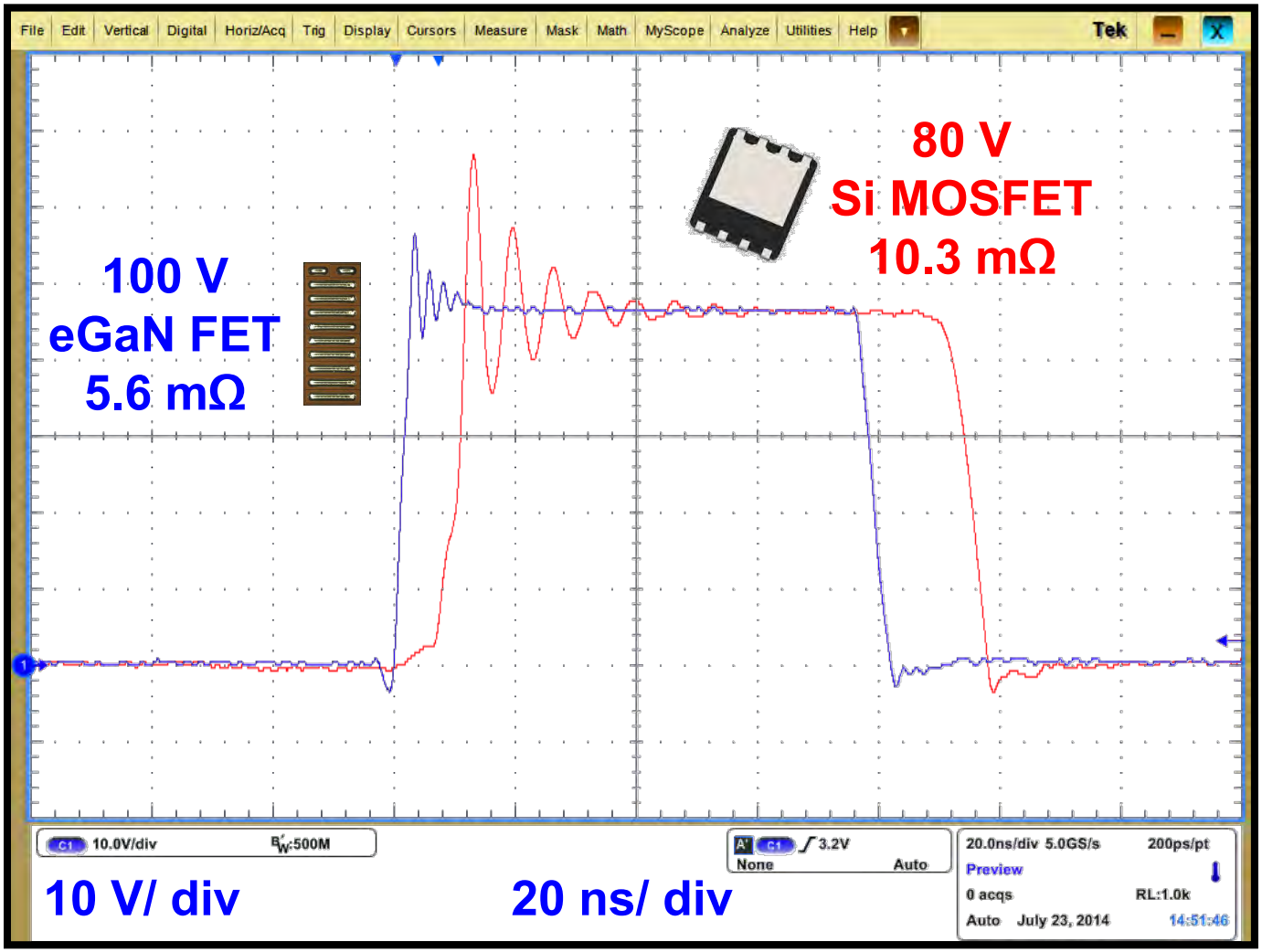



EPC2001 = 100 V, 5.6 mΩ typ.

BSC057N08 = 80 V, 4.7 mΩ typ.

# Switching Comparison

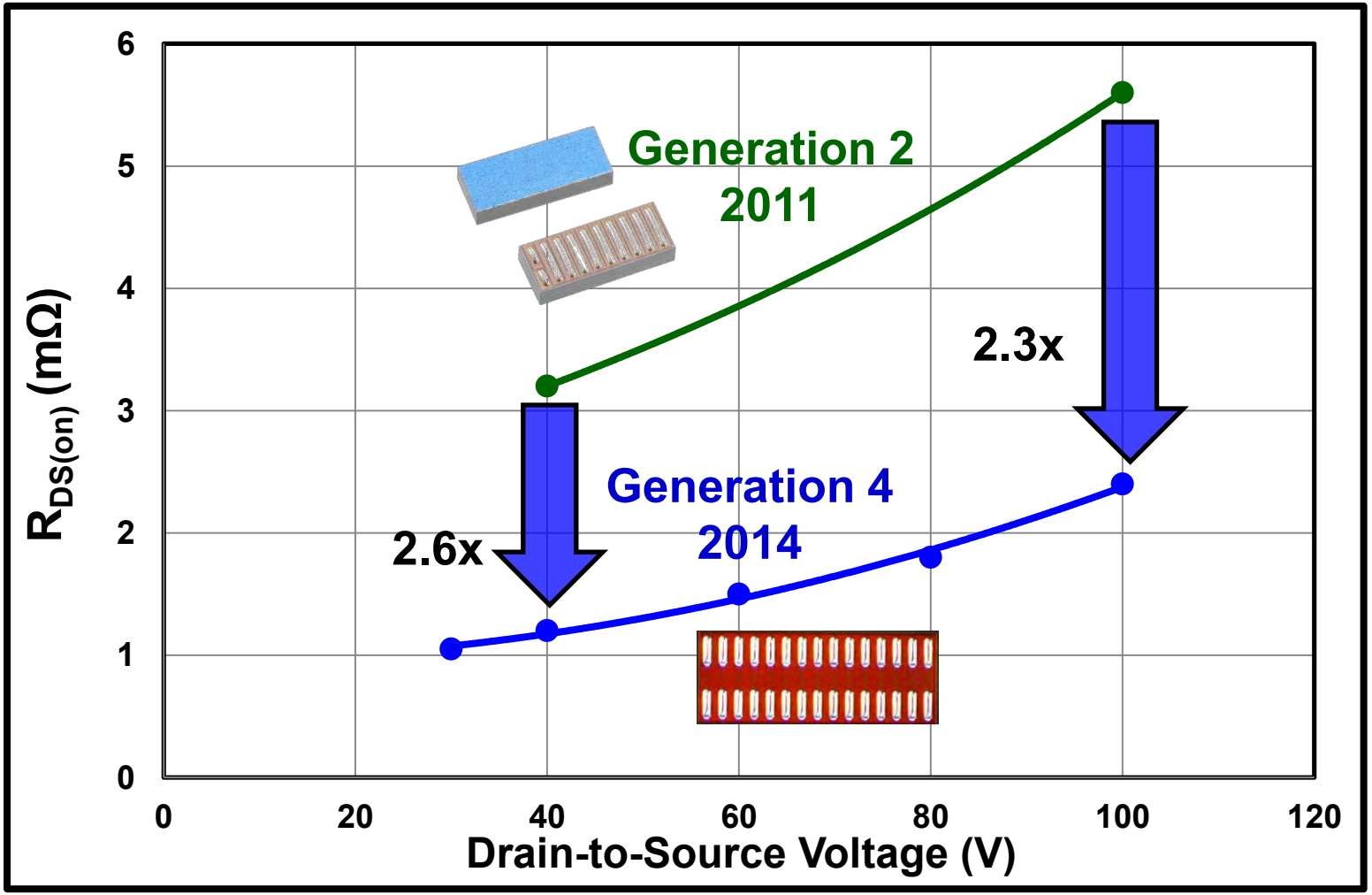





$V_{IN}$=48 V $V_{OUT}$=1 V $I_{OUT}$=10 A $f_{sw}$=300 kHz L=10 µH eGaN FET T/SR: 100 V EPC2001
MOSFET T/SR: 80 V BSZ123N08NS3G

# GaN Improvements

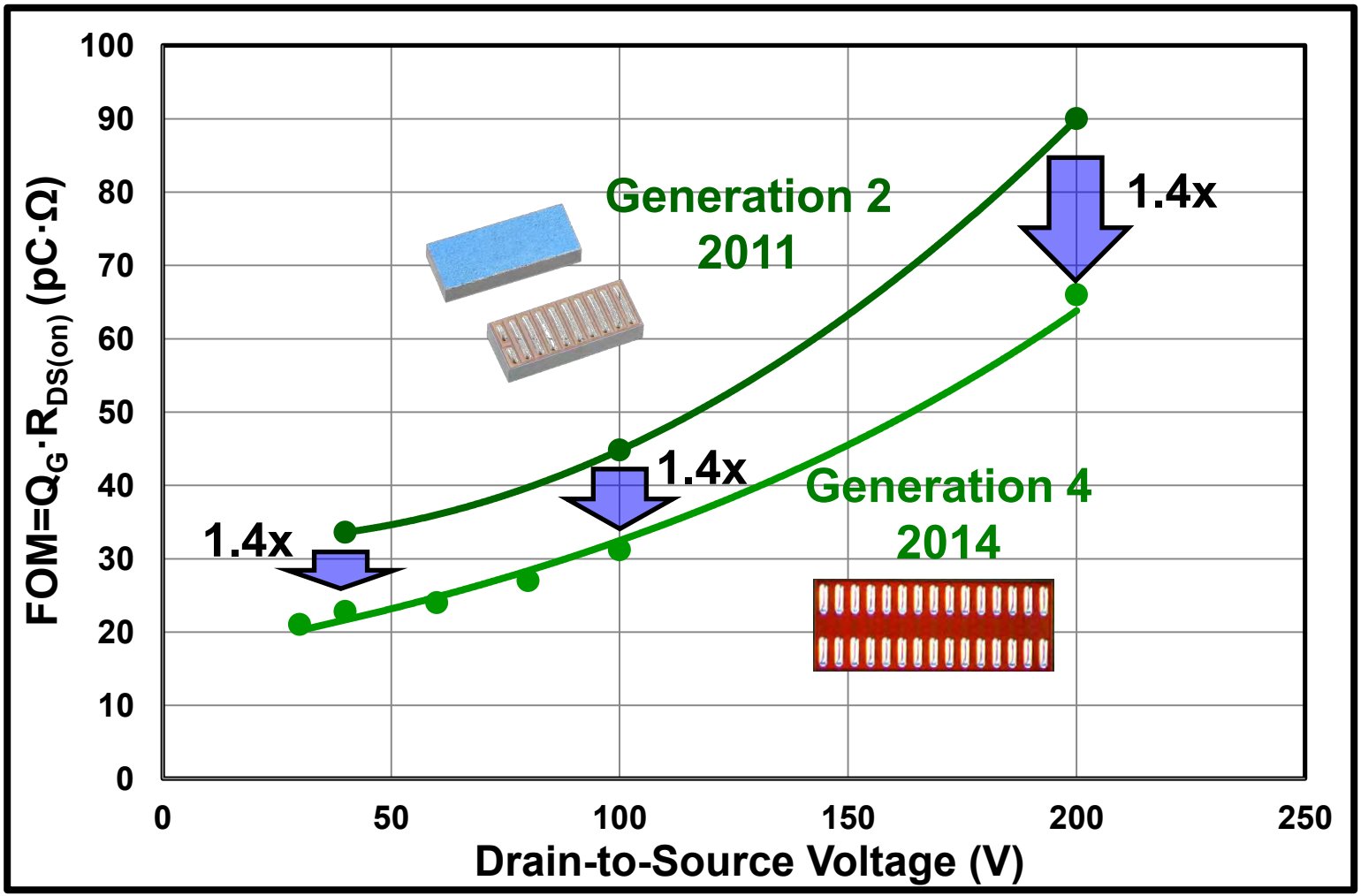





$V_{GS}$=5 V

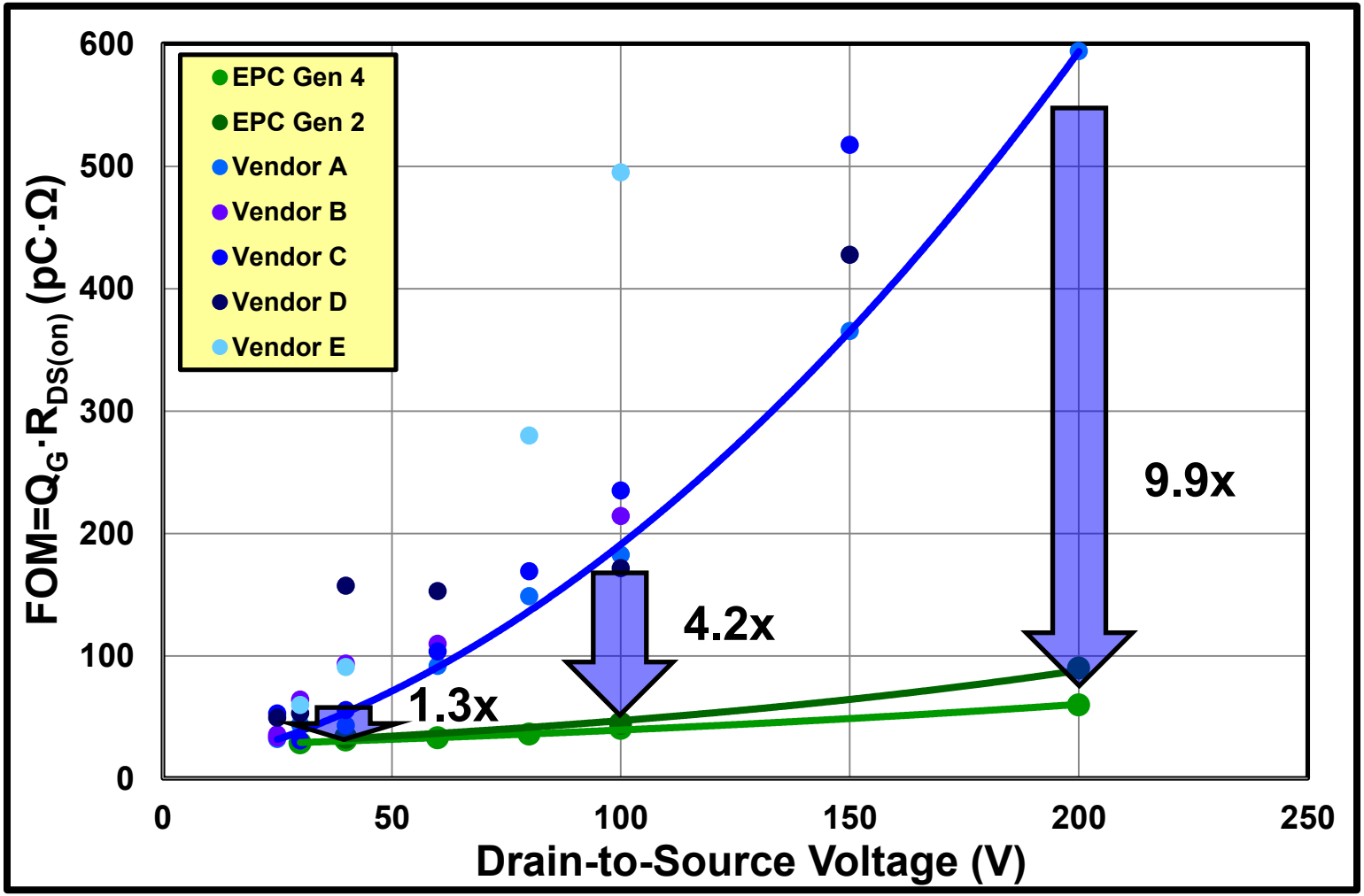
# Gate Charge FOM





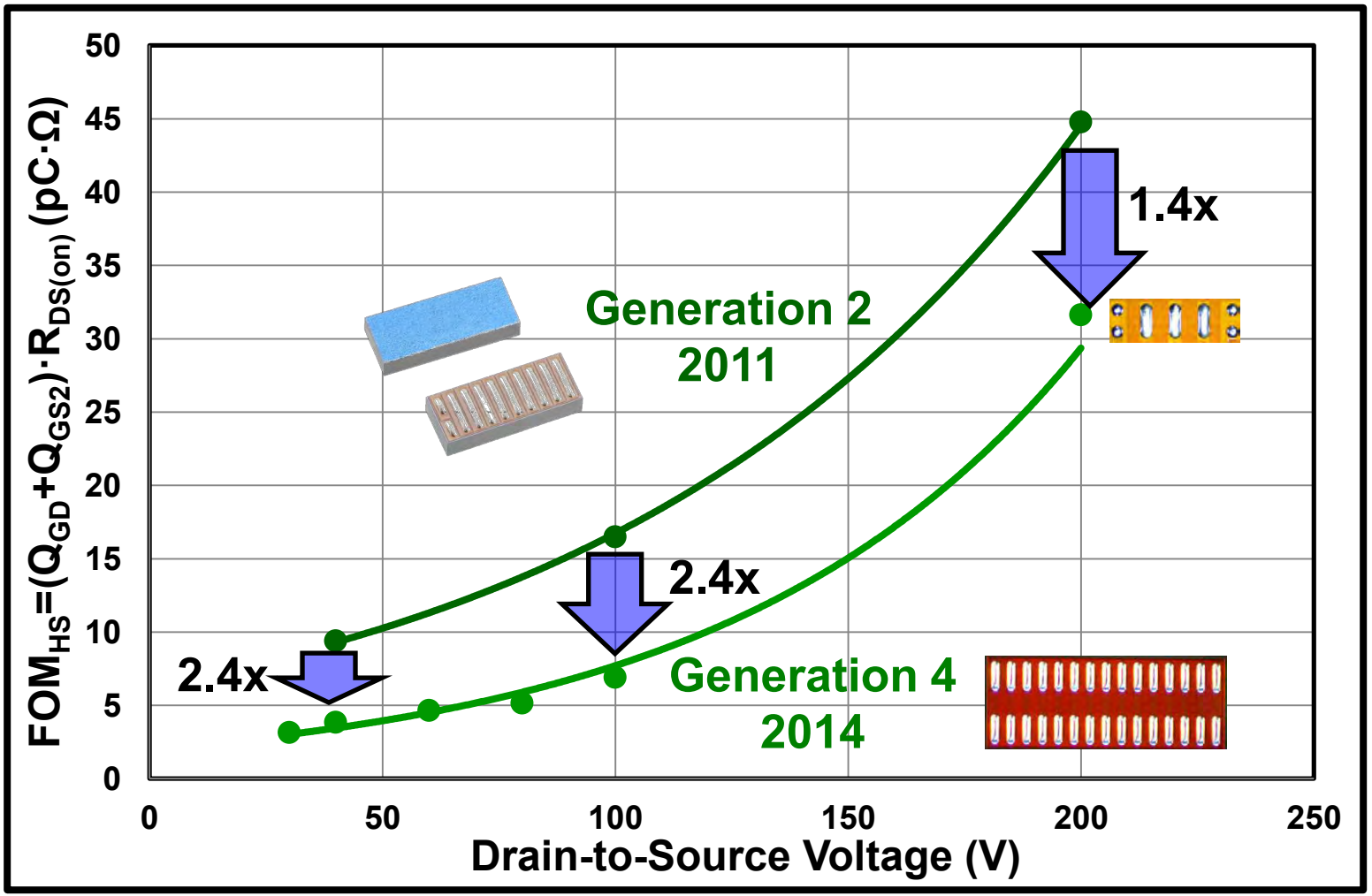
# Gate Charge Figure of Merit





# Hard Switching FOM

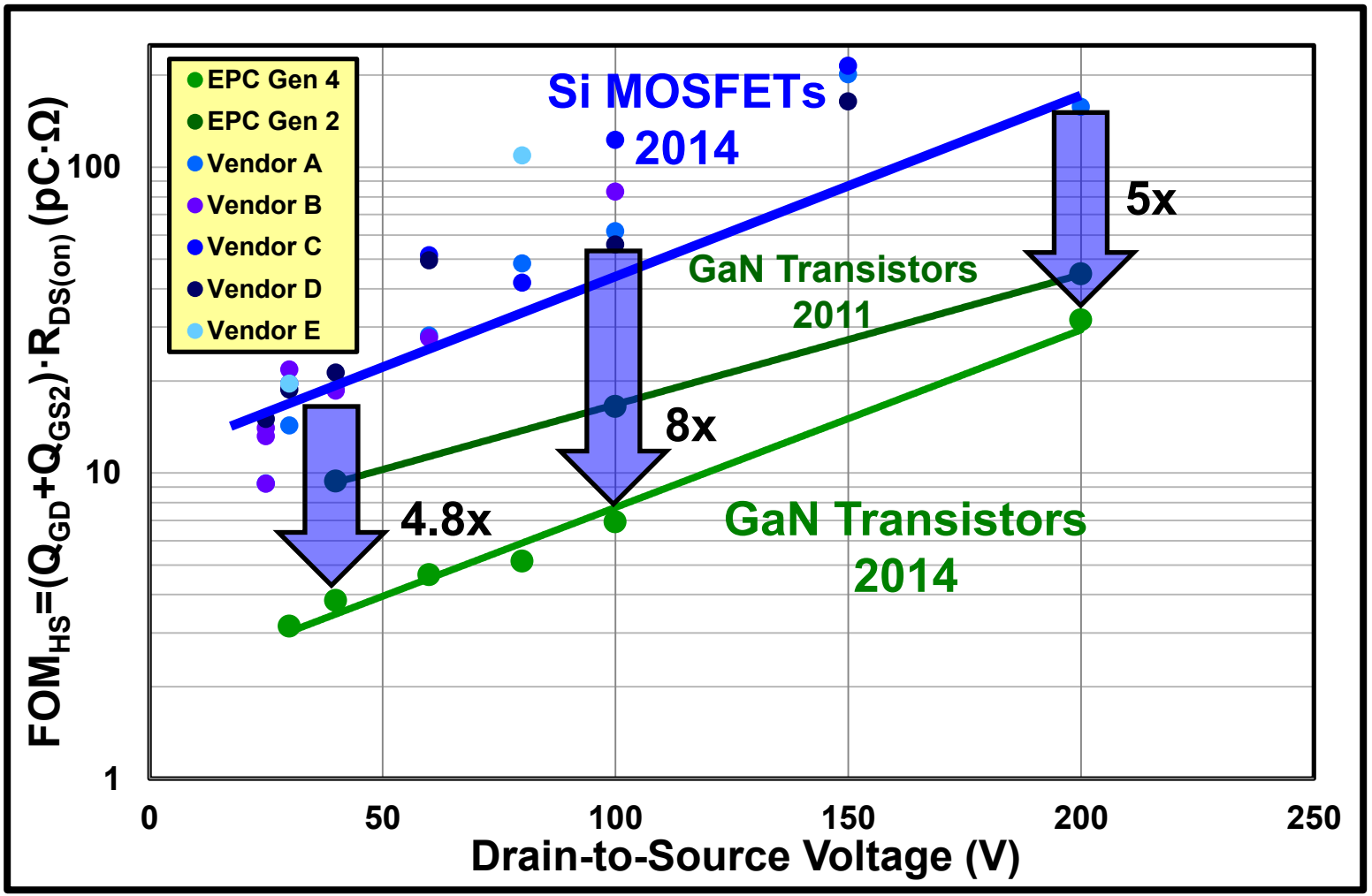





$V_{DS}=0.5\cdot V_{DSS}$, $I_{DS}=20$ A

# Hard Switching FOM

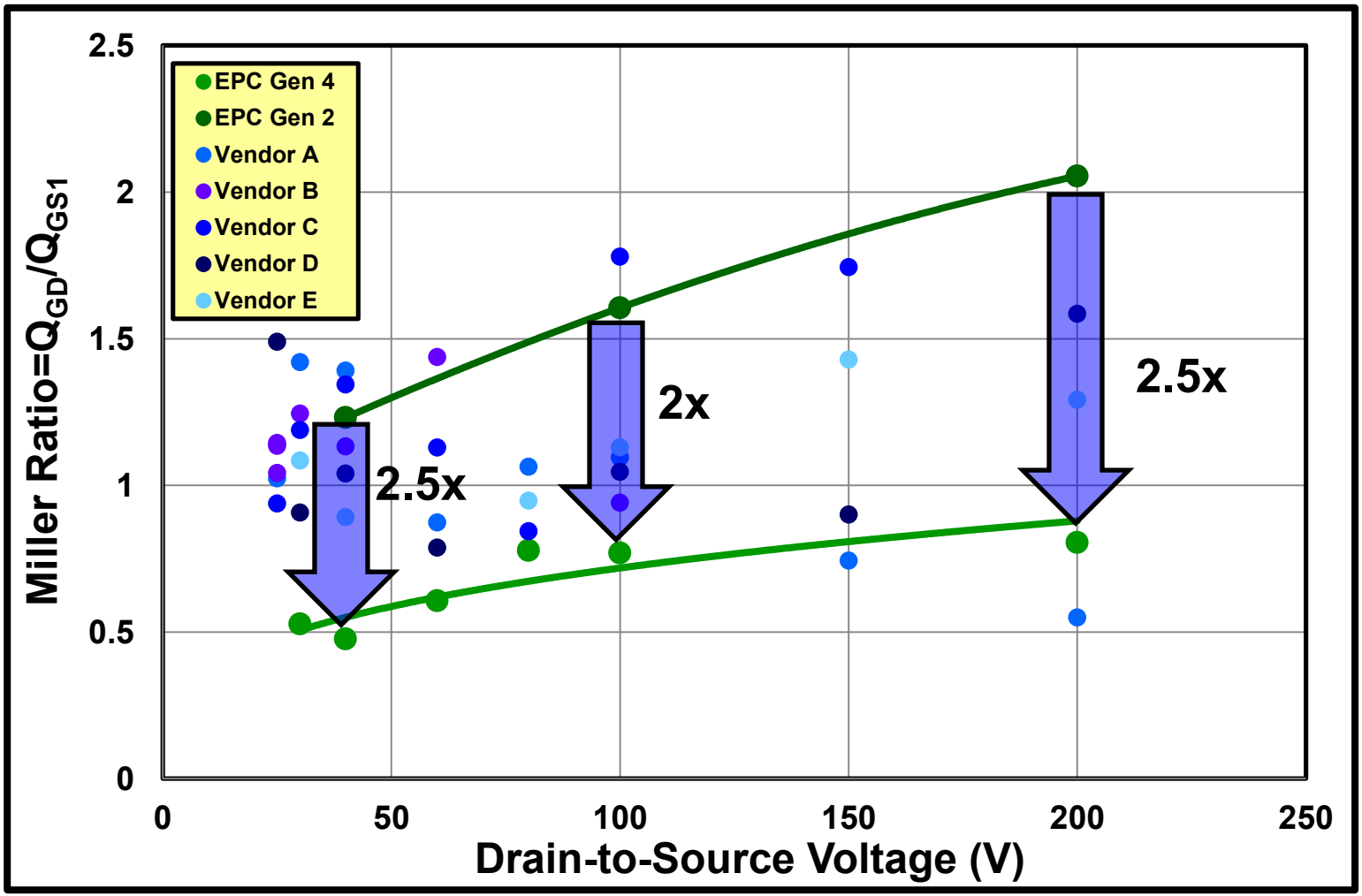





$V_{DS}$=0.5·$V_{DSS}$, $I_{DS}$=20 A

# Miller Ratio

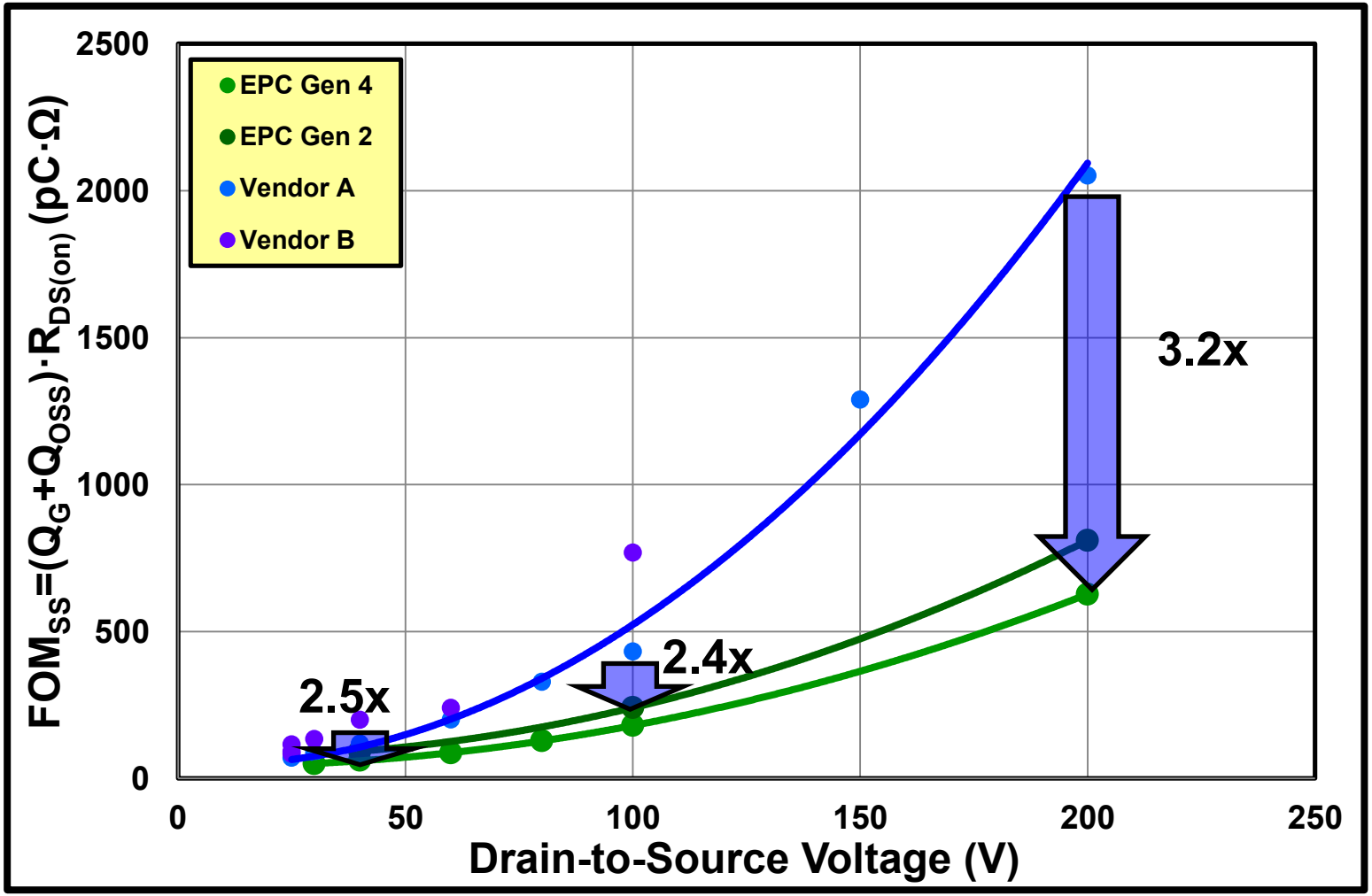





$V_{DS}$=0.5·$V_{DSS}$, $I_{DS}$=20 A

# Soft-Switching Figure of Merit






$V_{DS}=0.5 \cdot V_{DSS}$

# eGaN FET Loss Mechanisms



**Like** A MOSFET

- $I^2R$ Conduction Loss
- Capacitive Switching Losses
- Gate Drive Losses
- V×I Switching Loss

**Not Like** A MOSFET

- High Reverse Conduction Loss
- No Body Diode Reverse Recovery Loss

Can be much, much better than comparable silicon MOSFET

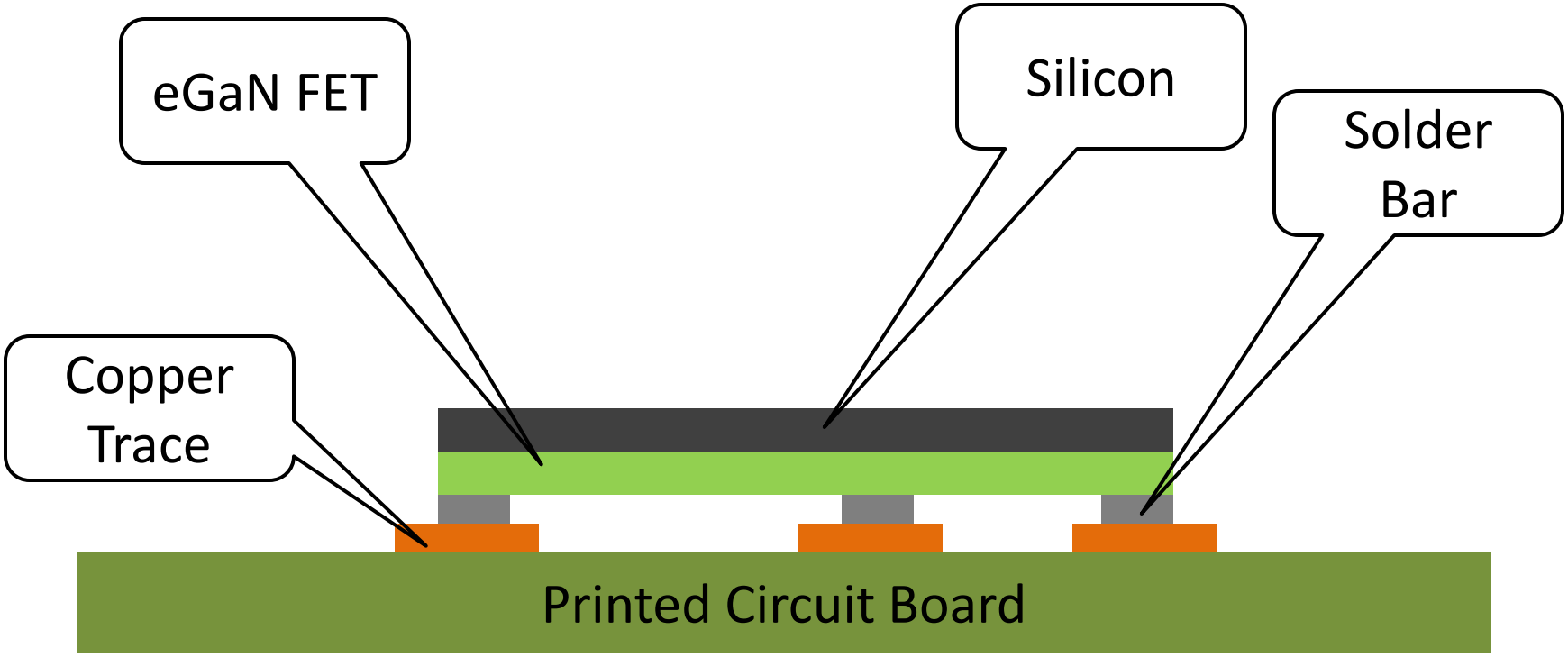
# Package Wish List



- Low parasitic resistance
- Low parasitic inductance
- Low thermal resistance
- Small size
- Low cost

# Flip-Chip LGA Construction





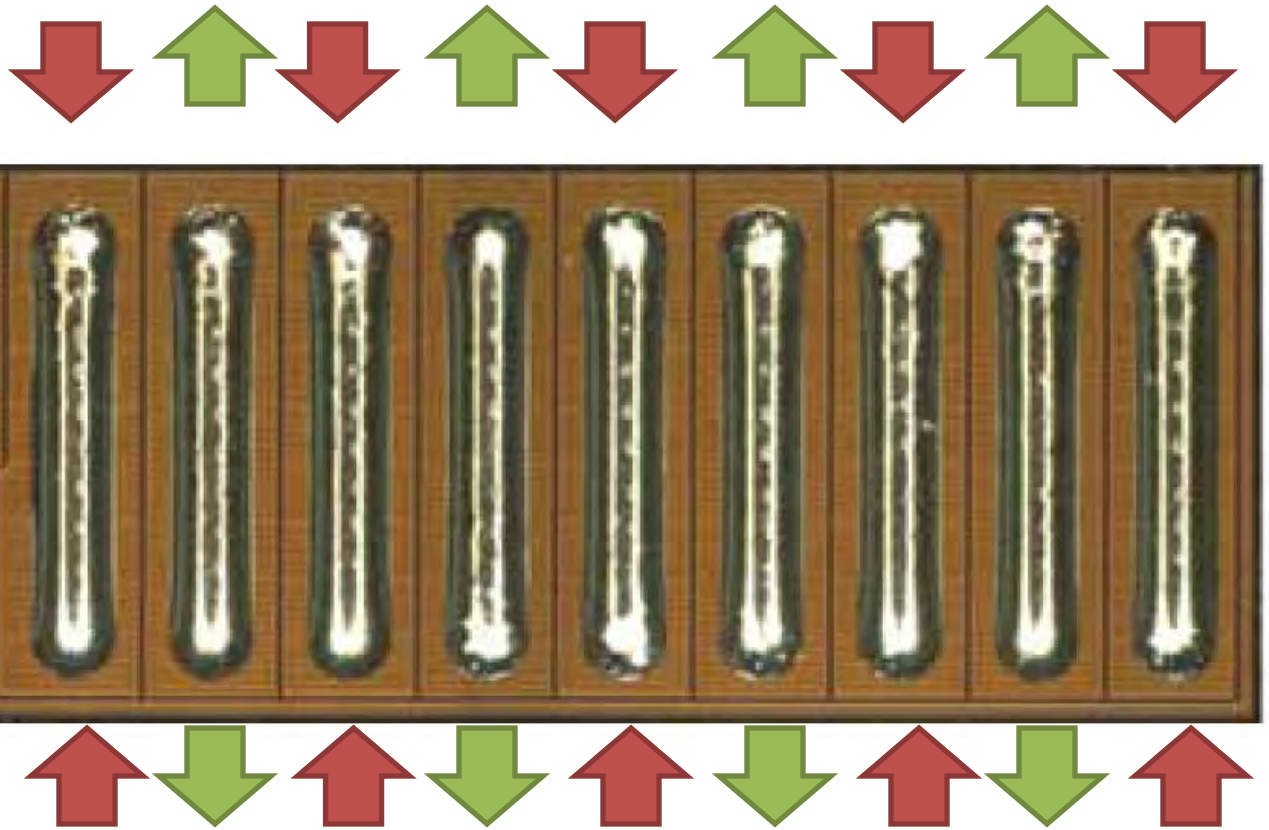

Absolute minimum lead resistance and inductance!

# LGA Construction



Drain Contacts

Interleaving to reduce layout inductance



Substrate

Gate

Source Contacts

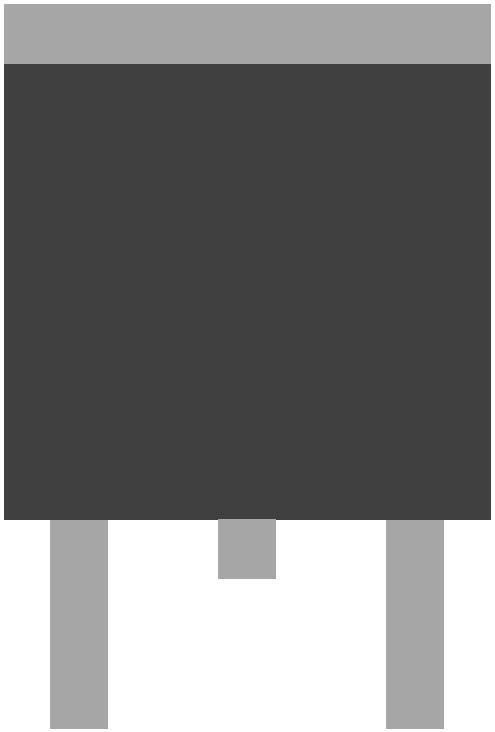
# Size Comparison – 200 V



D-PAK

eGaN FET

5.76 mm²



65.3 mm²

Drawn To Scale

# Design Basics

# Design Basics Agenda

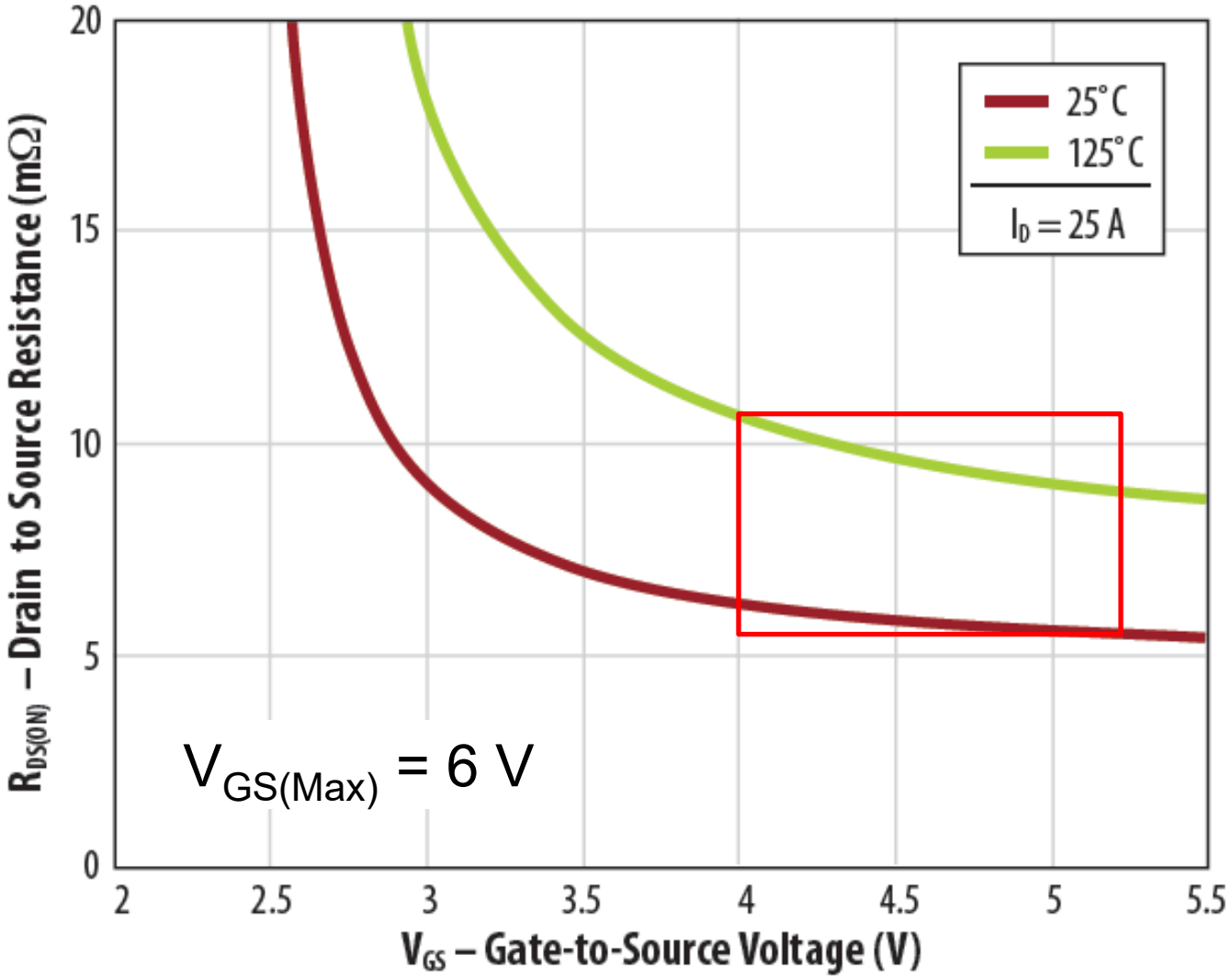


- Requirements for:
  - Gate Driver
  - Dead-time
  - Layout
  - Paralleling
  - Thermal
  - Measurement

# Gate Drive

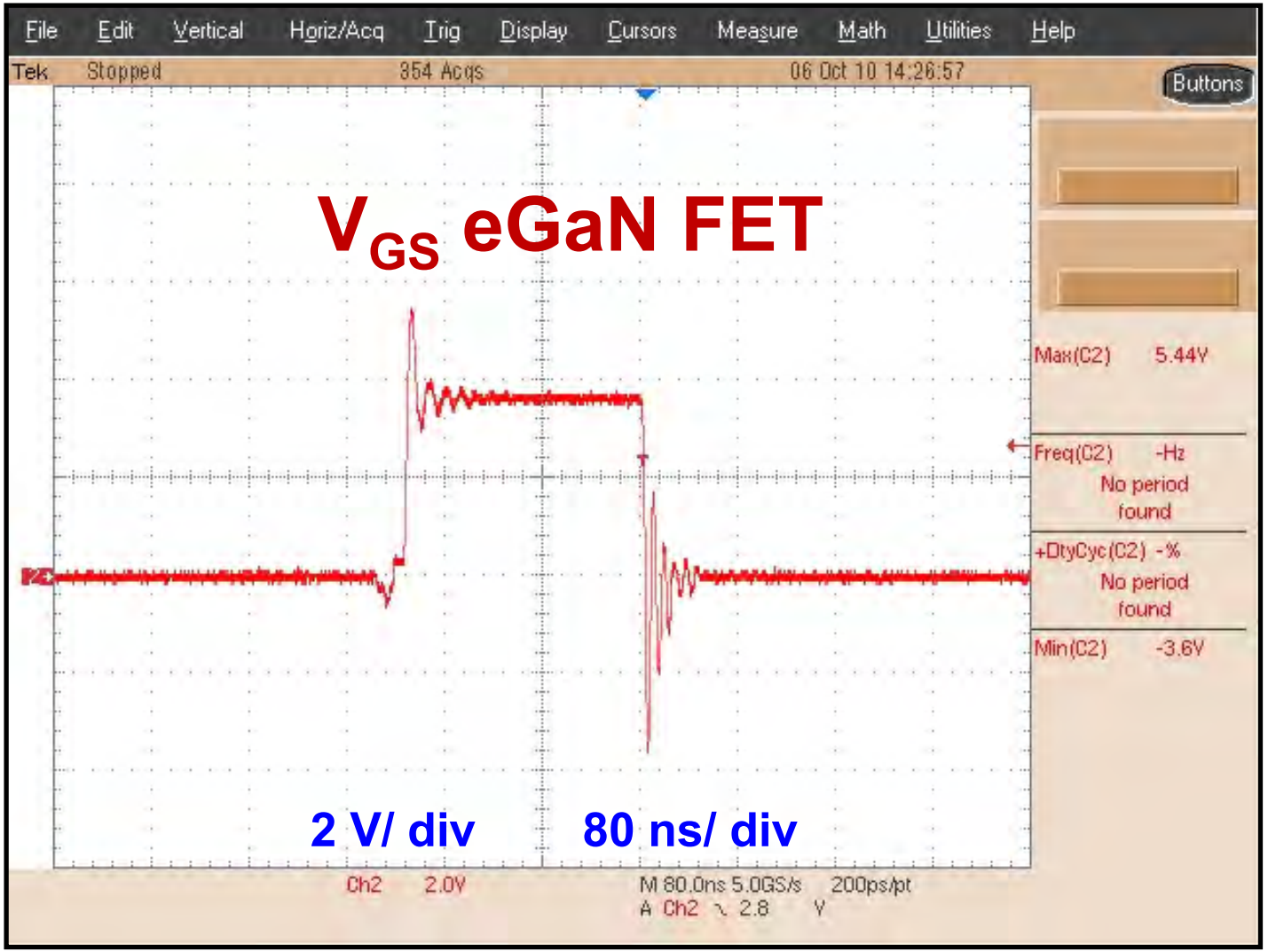
# Low $V_{GS(on)}$ Overhead





# Minimizing Overshoot



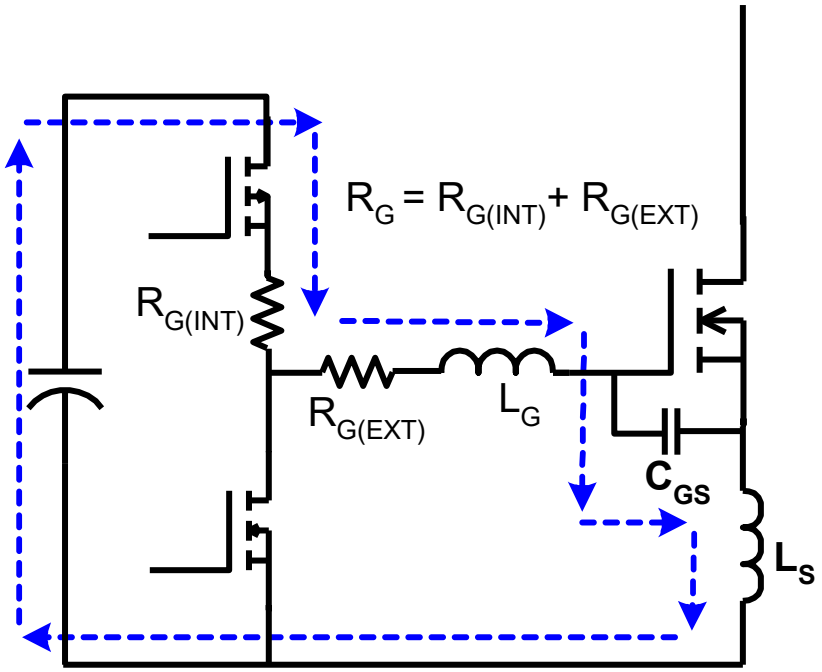


# eGaN FET Drive Requirements



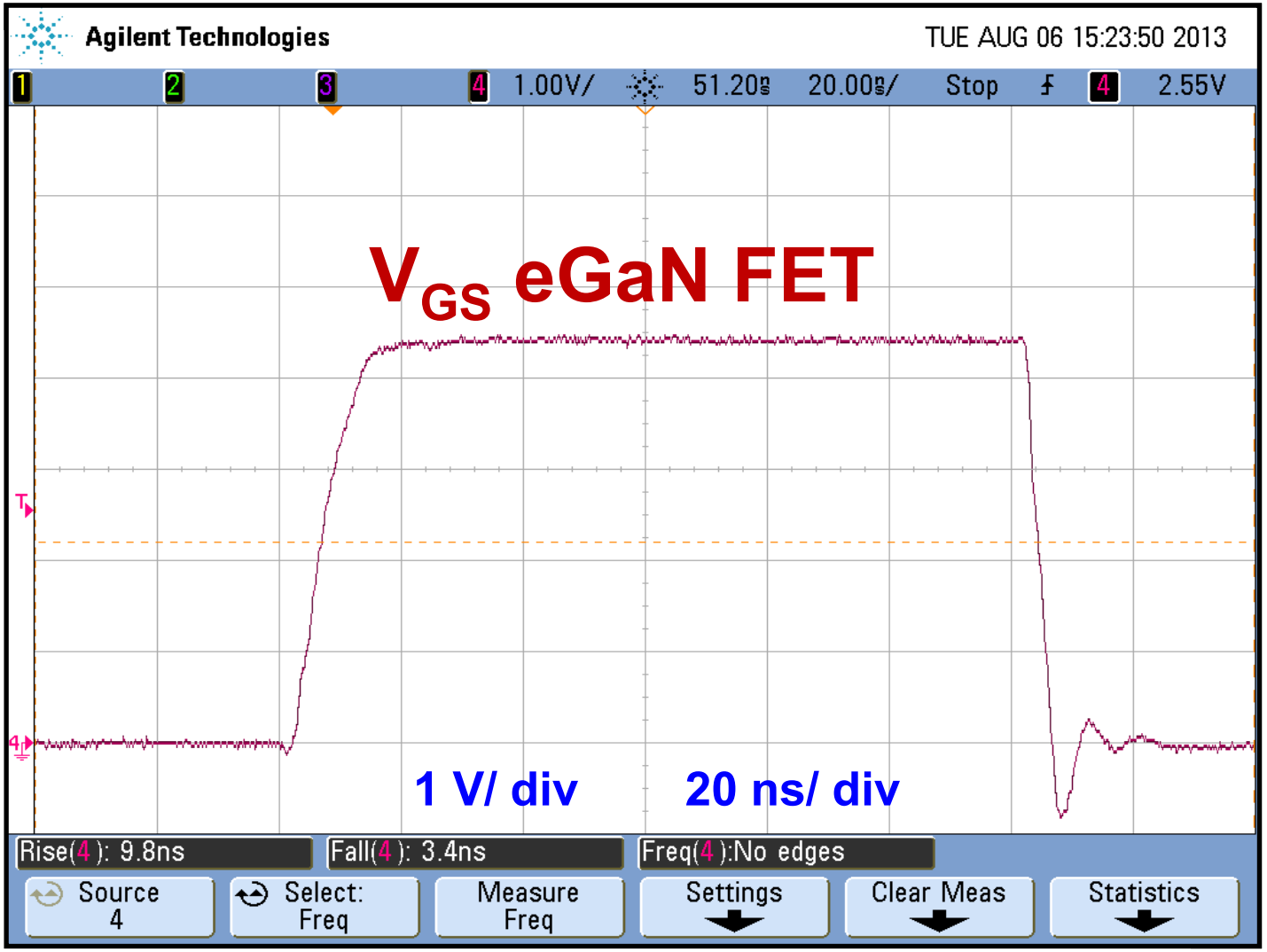
To avoid overshoot:

$$R_G \geq \sqrt{\frac{4(L_G + L_S)}{C_{GS}}}$$



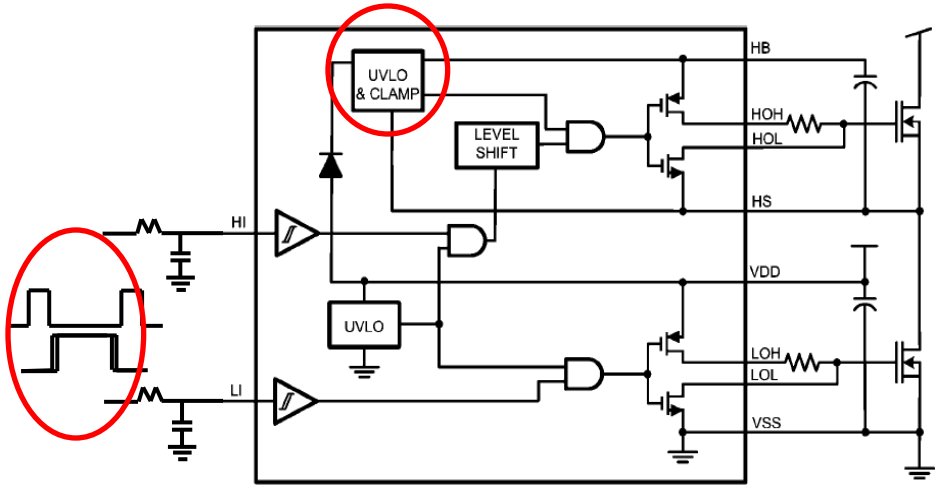

- Minimize gate loop inductance
- Separate source and sink transistors allowing for separate drive paths

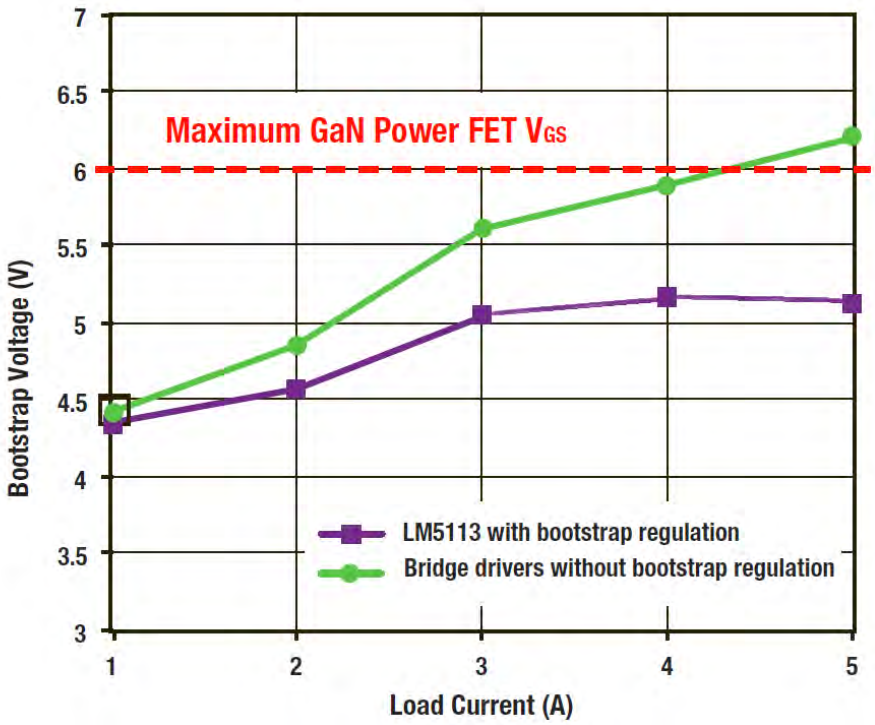
# Minimizing Overshoot



# eGaN FET Driver IC





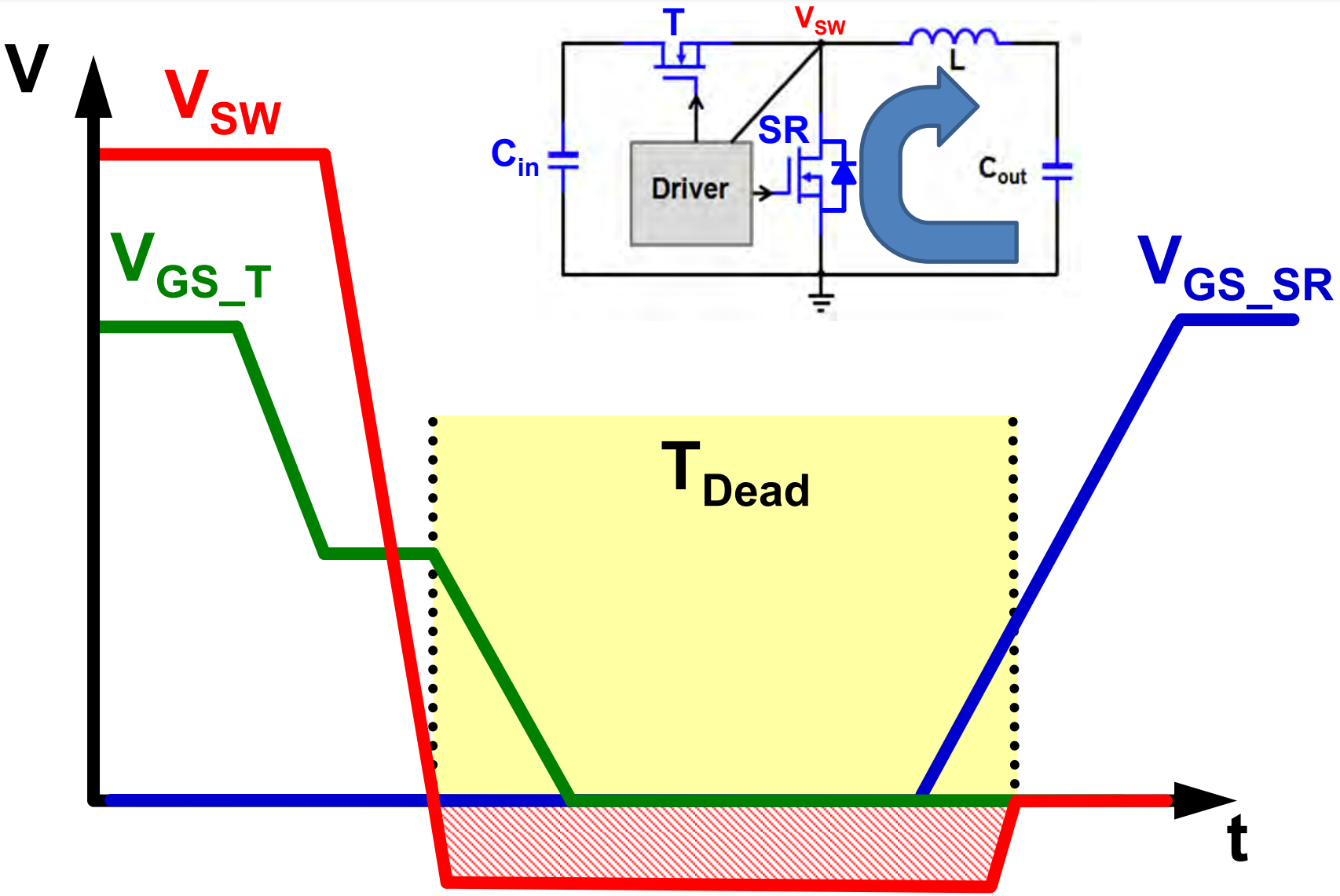

- Bootstrap clamp limits (HS) supply
- Separate inputs allow accurate, dead-time management
- Optimized drive impedance

Reference: Texas Instruments, "Gate Drivers for Enhancement Mode GaN Power FETs 100 V Half-Bridge and Low-Side Drivers Enable Greater Efficiency, Power Density, and Simplicity," SNVB001

# Dead-time Requirements

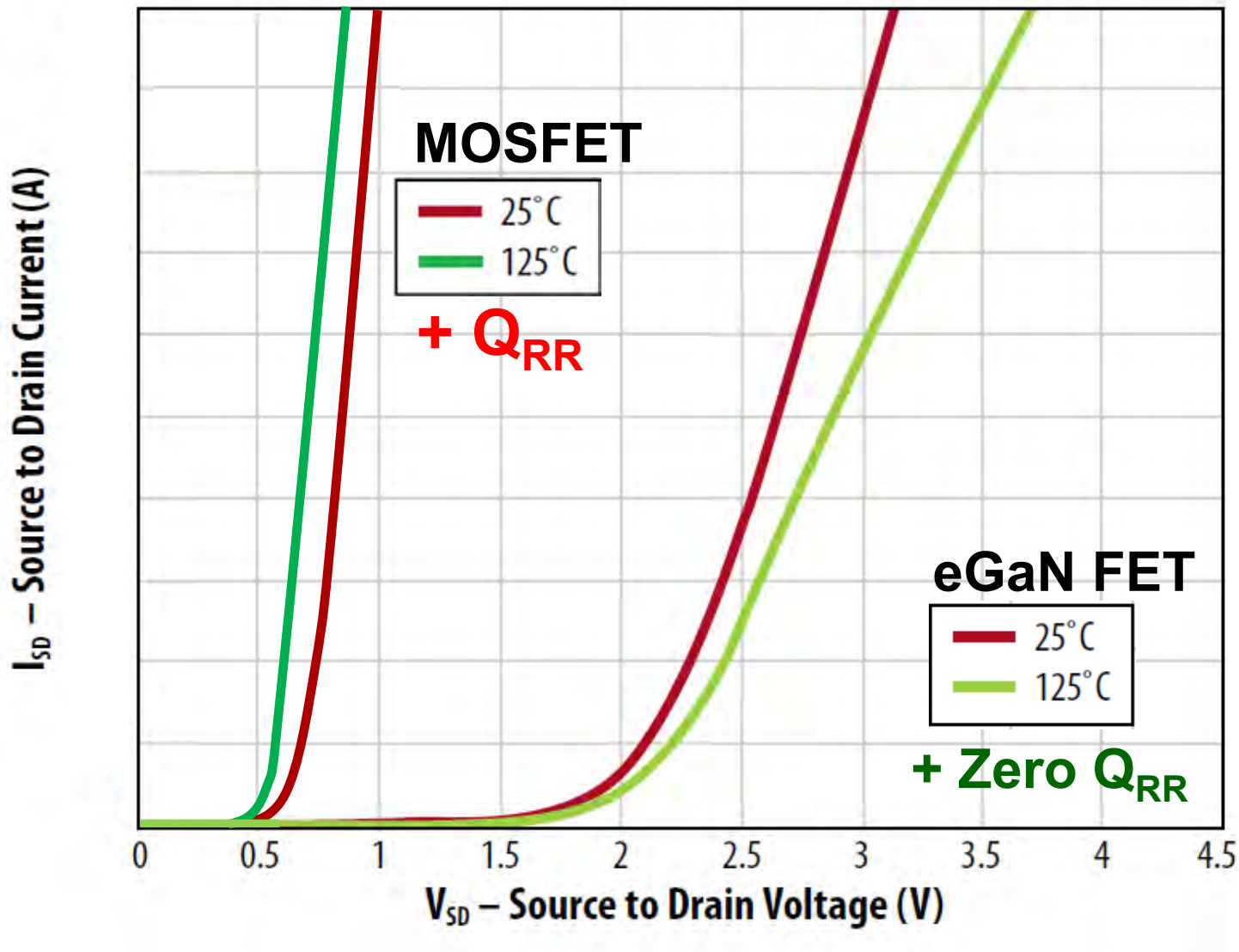
# Reverse Conduction Period





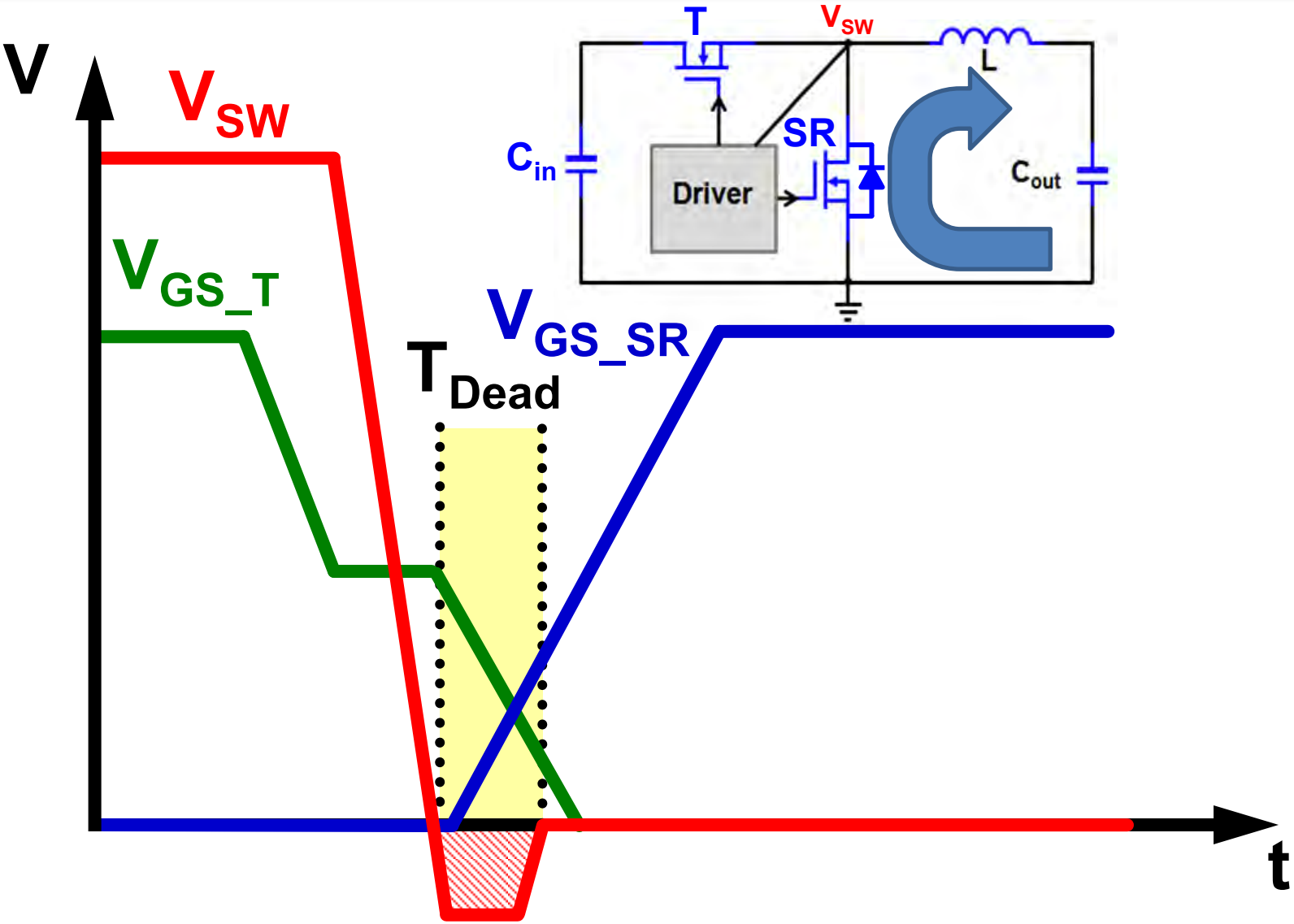
# eGaN FET Reverse Conduction





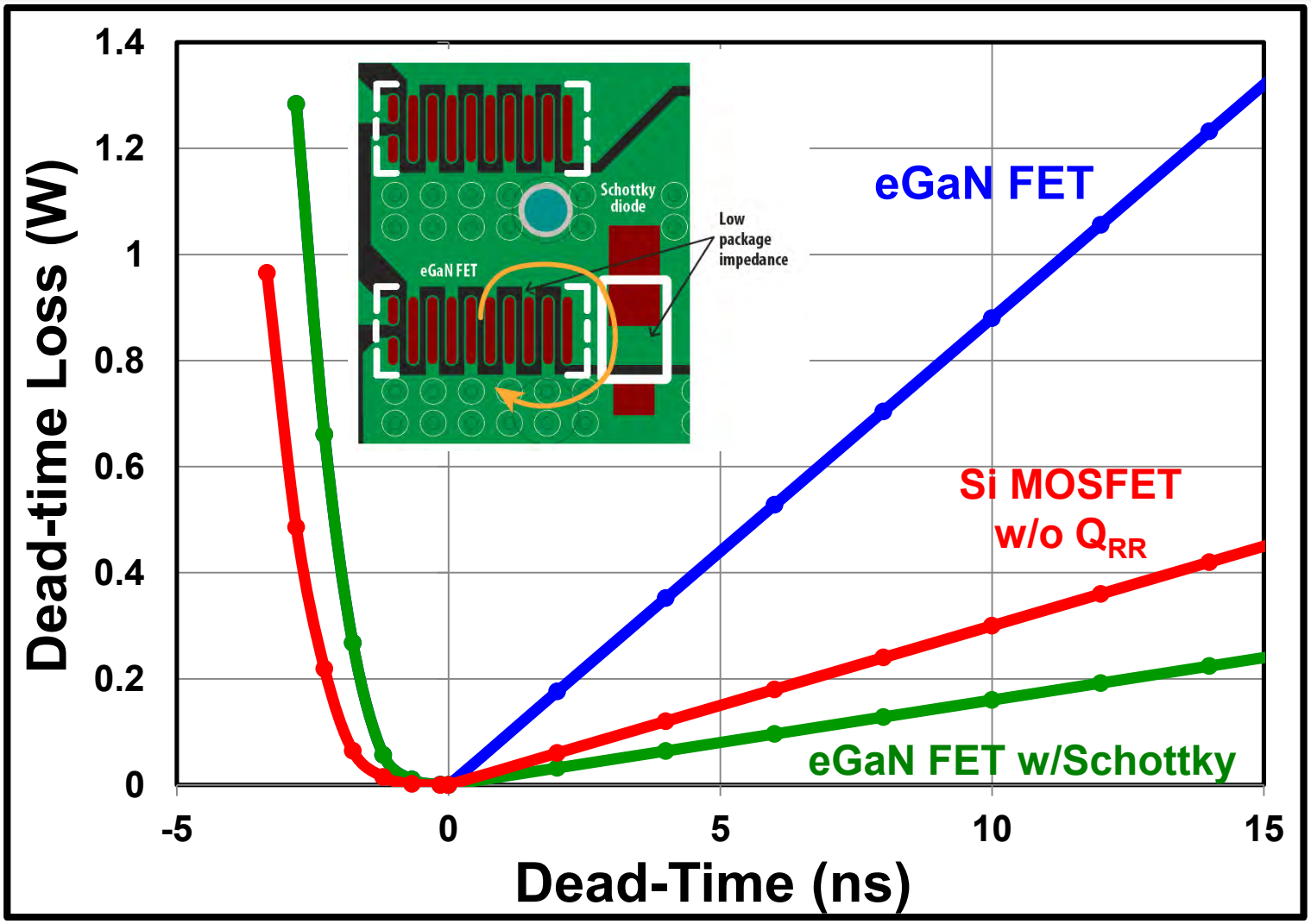
# Reverse Conduction Period





# Impact of Dead-time

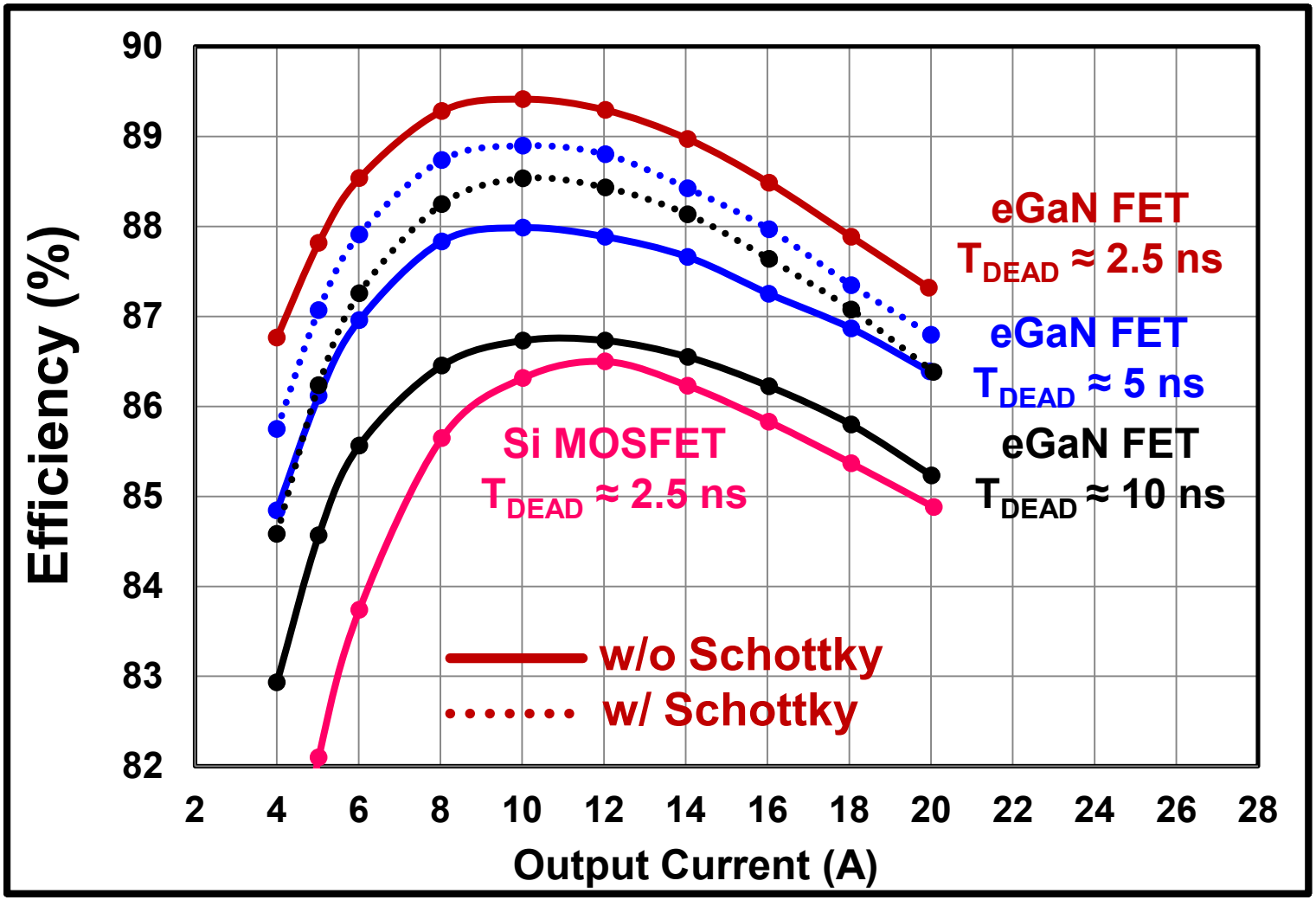





$V_{IN}$ =12 V, $V_{OUT}$ =1.2 V, $I_{OUT}$=20 A, and $f_{sw}$ =1 MHz

# Impact of Dead-time

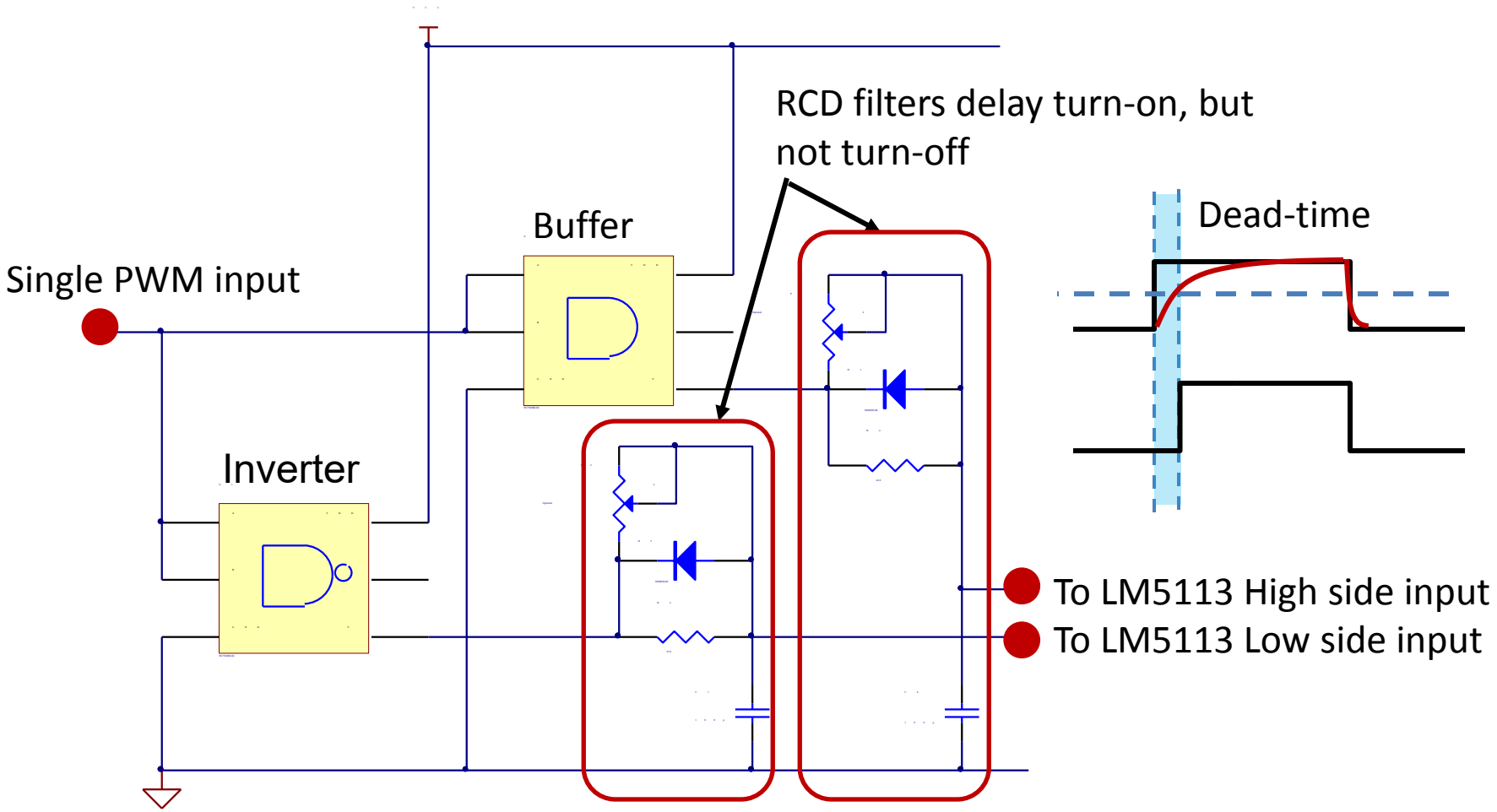





$V_{IN}$ =12 V, $V_{OUT}$ =1.2 V, and $f_{sw}$ =1 MHz

# Fixed Dead-time Implementation



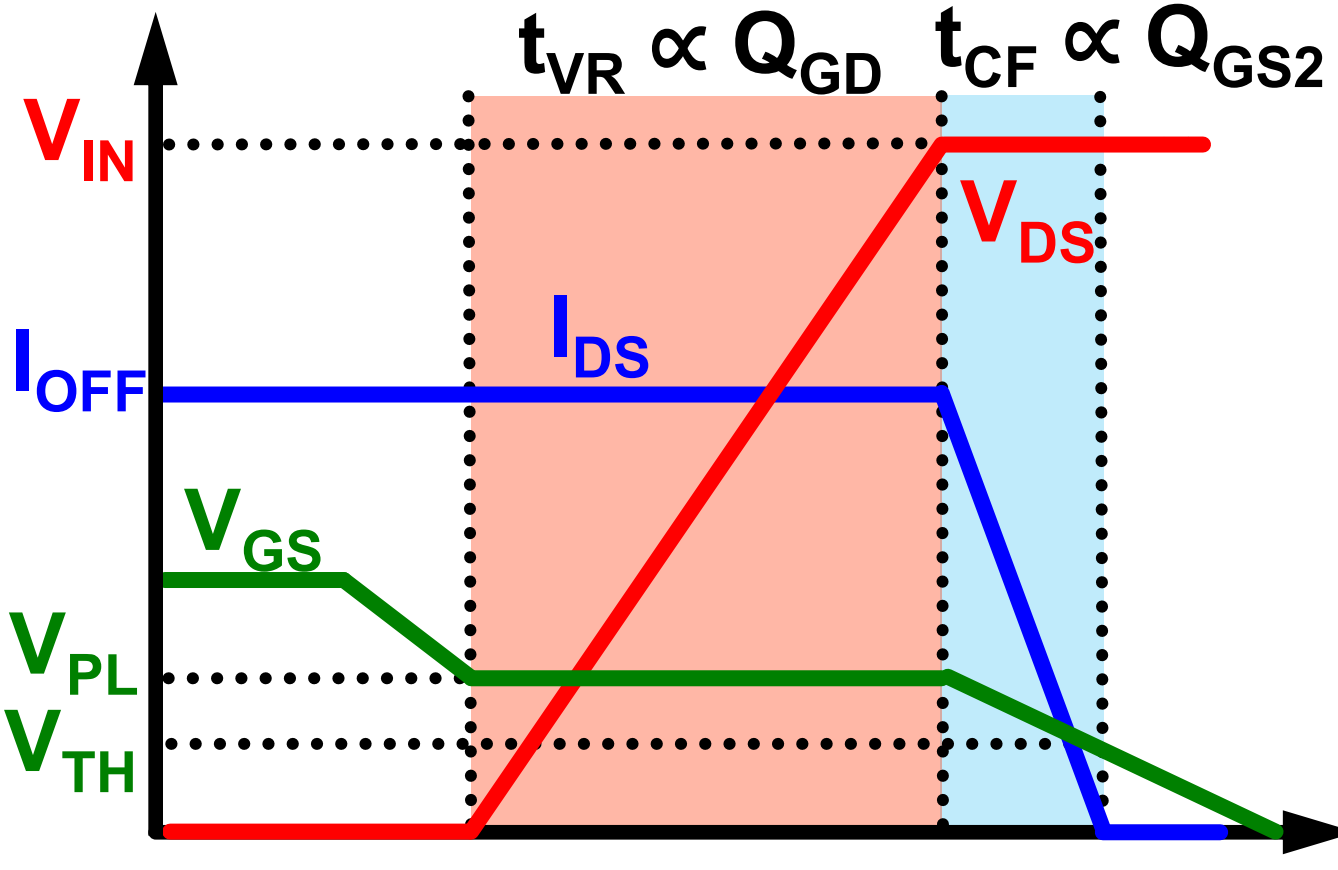



Used on all EPC90XX boards

# Layout

# Ideal Hard Switching



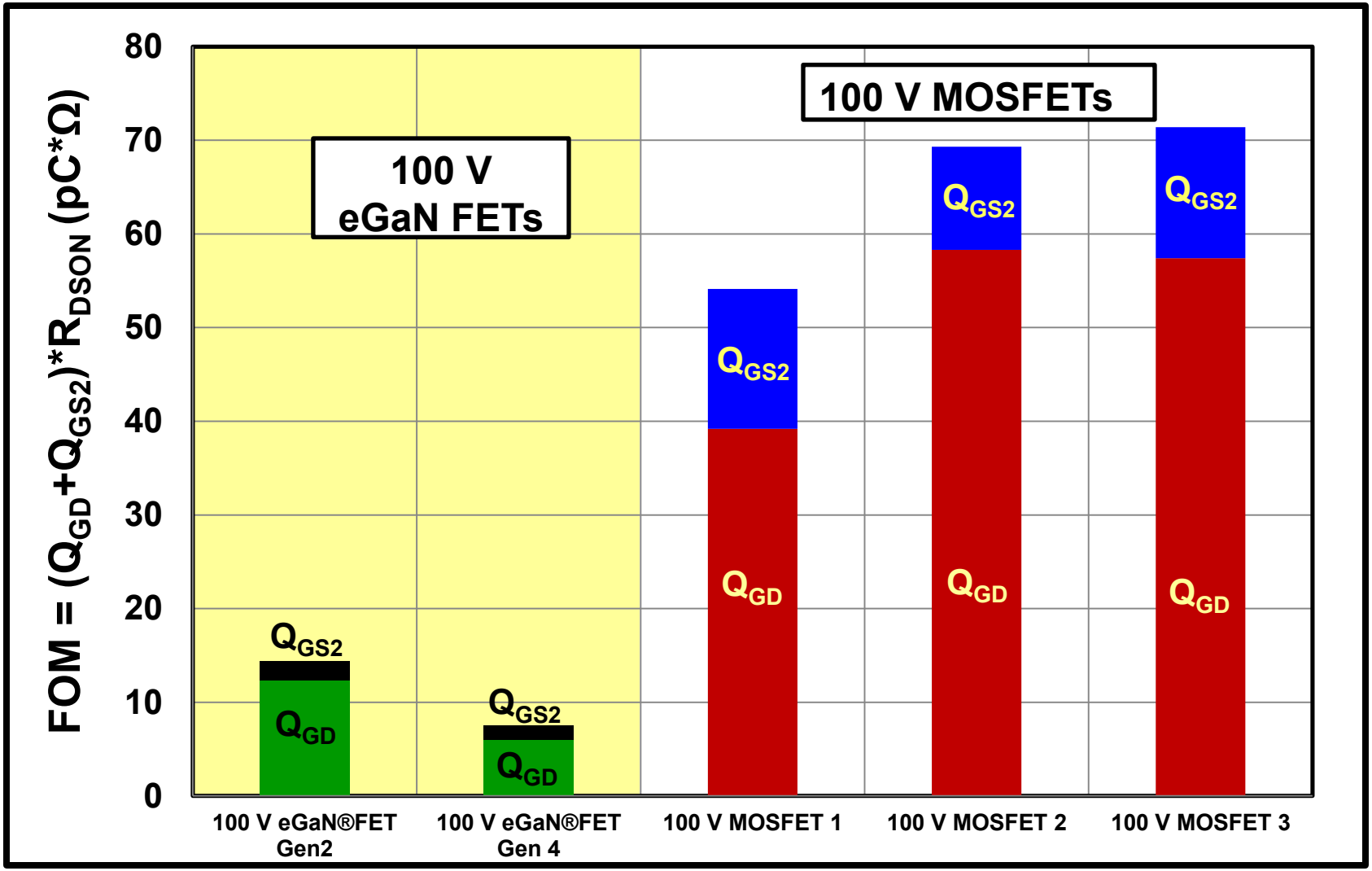



$$P_{t_{VR}} \approx \frac{V_{IN} * I_{OFF} * Q_{GD}}{2 * I_G}$$

$$P_{t_{CF}} \approx \frac{V_{IN} * I_{OFF} * Q_{GS2}}{2 * I_G}$$

# 100 V Device Comparison

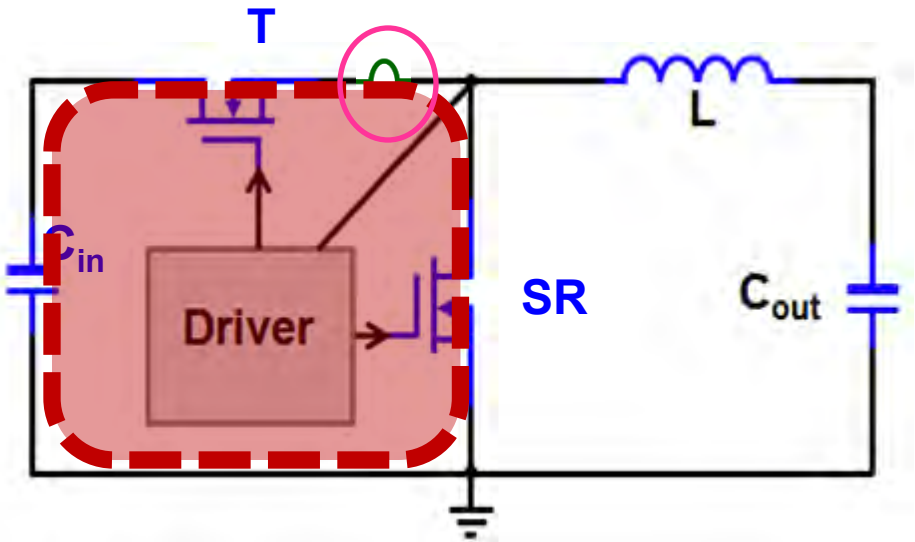





$V_{DS}$=0.5*$V_{DS}$, $I_{DS}$= 10 A

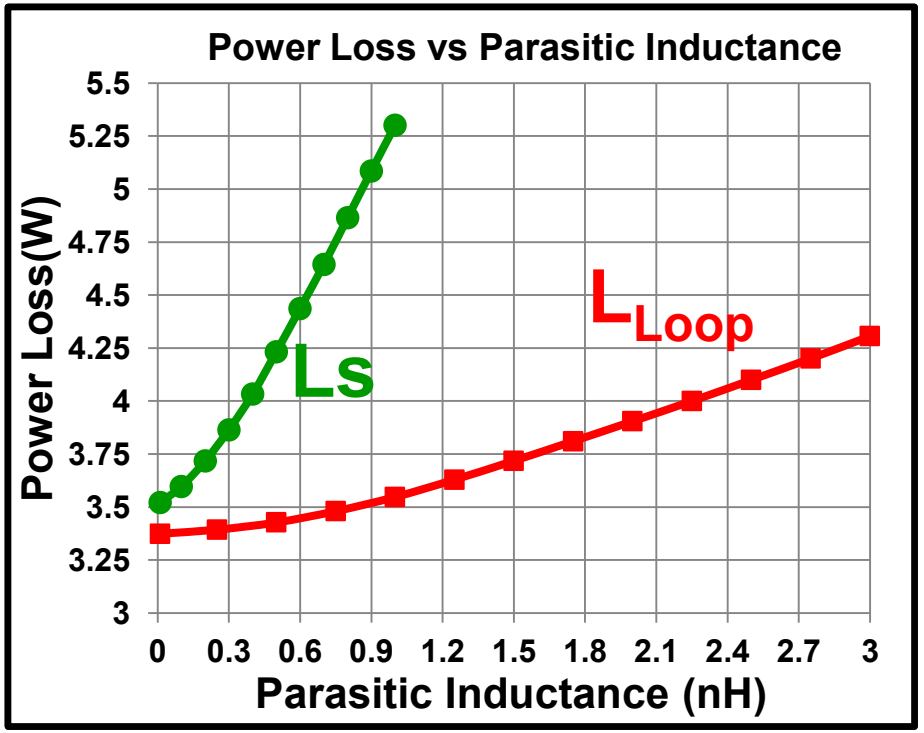
# Converter Parasitics





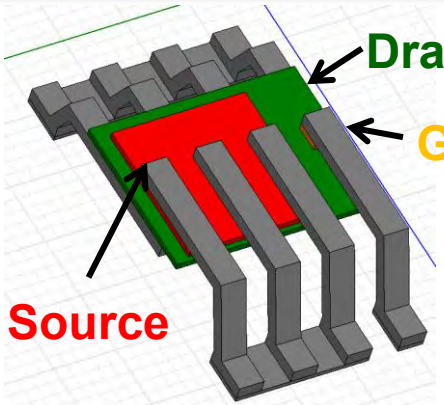

**$L_S$: Common Source Inductance**

**$L_{Loop}$: High Frequency Power Loop Inductance**

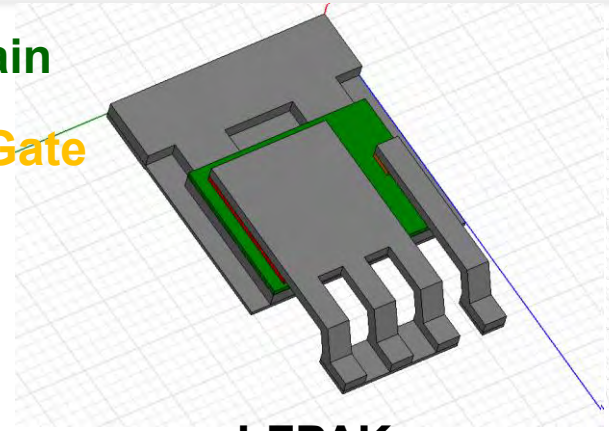



$V_{IN}$=12 V, $V_{OUT}$=1.2 V,
$f_{sw}$=1 MHz, $I_{OUT}$= 20 A

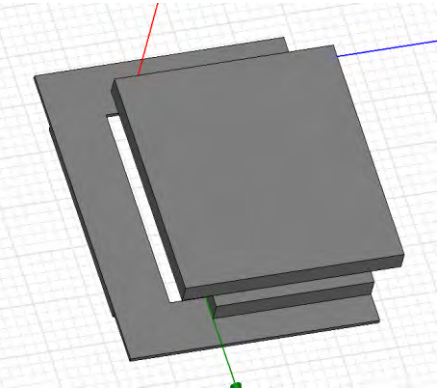
# Package Impact on Efficiency




SO-8

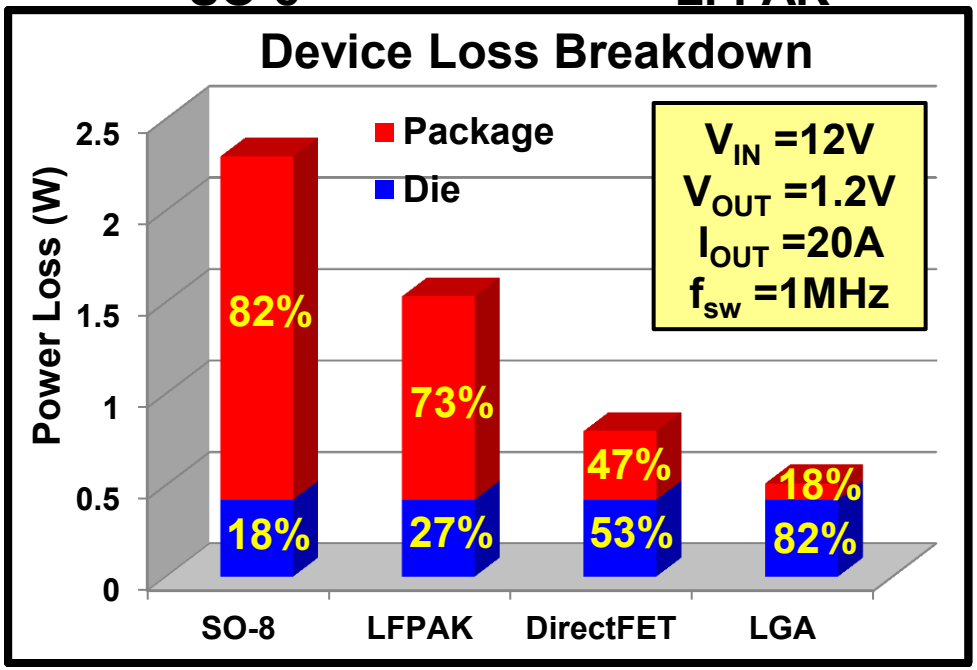


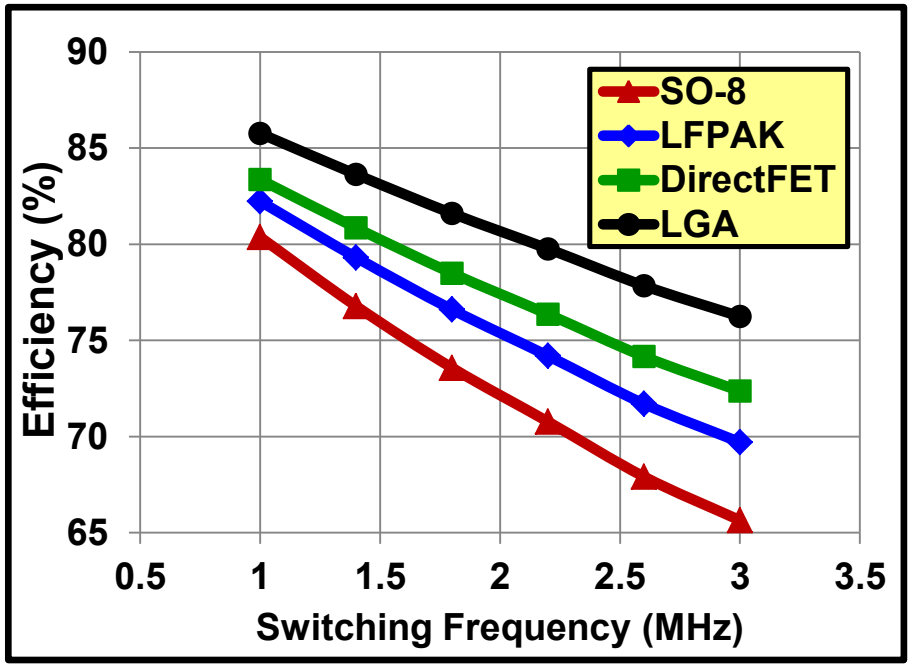
LFPAK



DirectFET

LGA eGaN FET

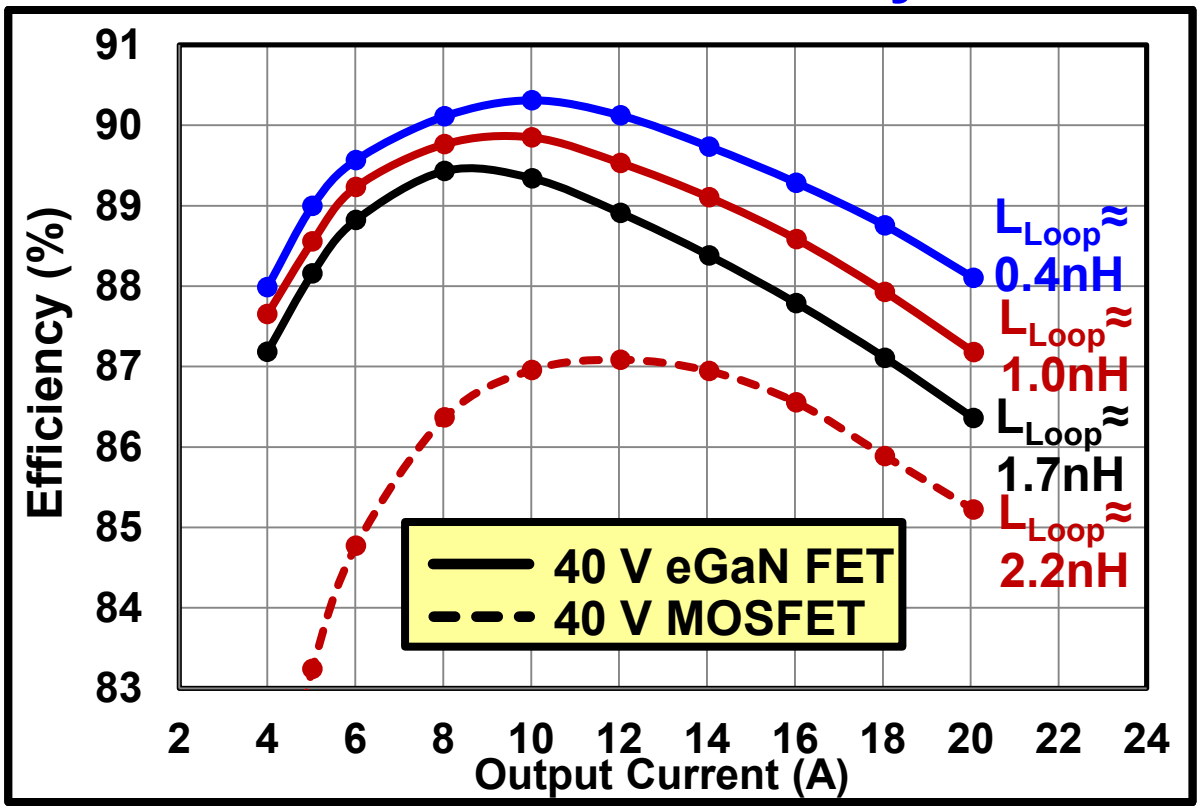


# Layout Impact on Efficiency

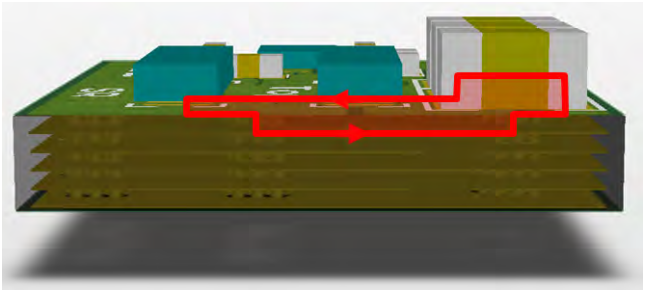


## Measured Efficiency




$V_{IN}$=12 V, $V_{OUT}$=1.2 V, $f_{sw}$=1 MHz, L=300 nH

## EPC Optimal Layout

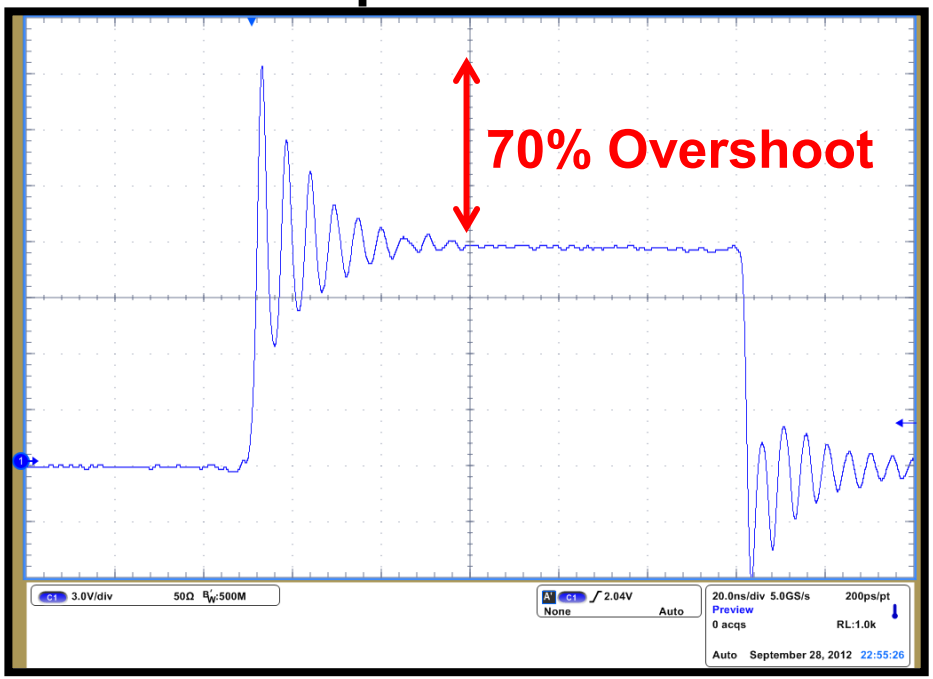


Ref: D. Reusch, J. Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter," APEC 2013

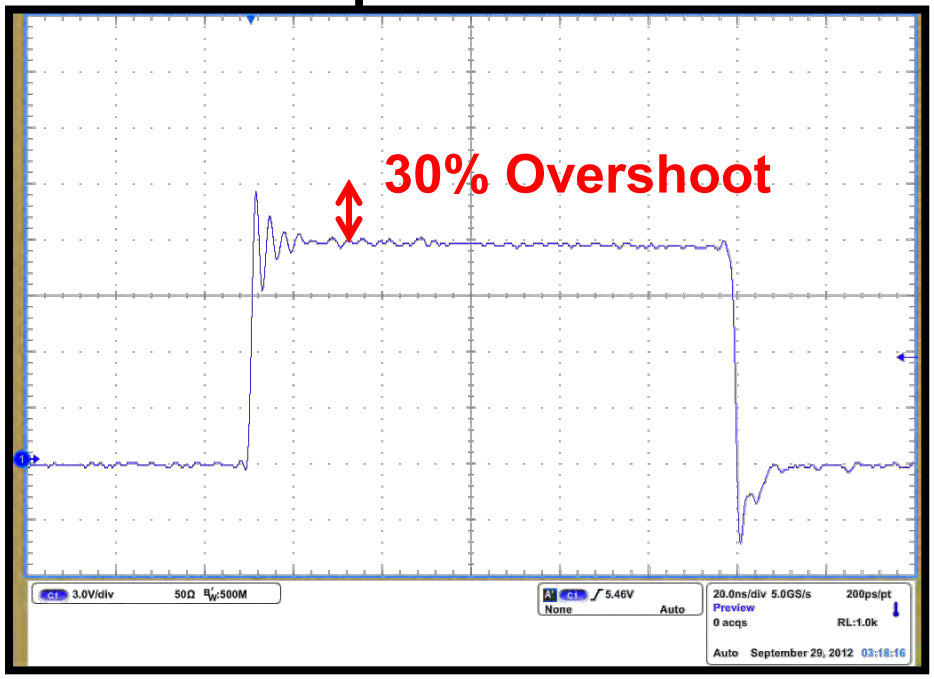
# Layout Impact on Peak Voltage



## $L_{Loop} \approx 1.0$ nH




## $L_{Loop} \approx 0.4$ nH




**Switching Node Voltage**

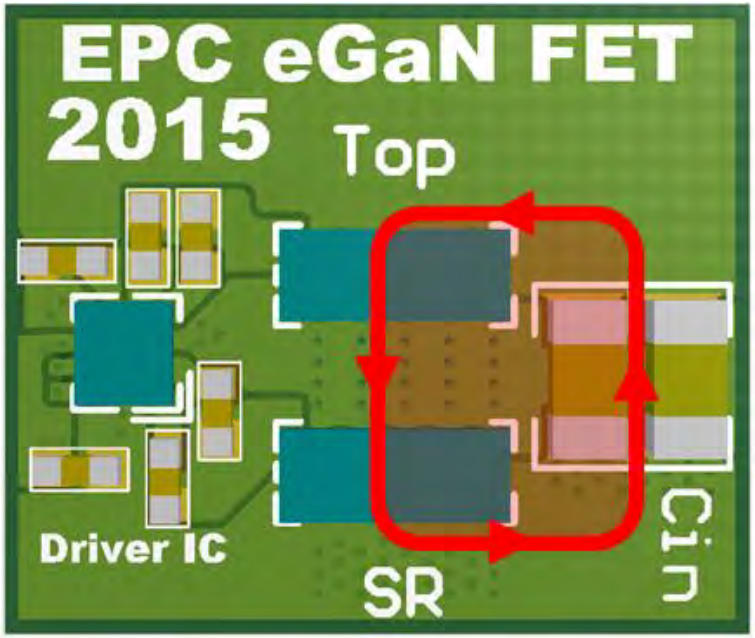
**$V_{IN}$=12 V $V_{OUT}$=1.2 V $I_{OUT}$=20 A**

**$f_{sw}$=1 MHz L=150 nH**

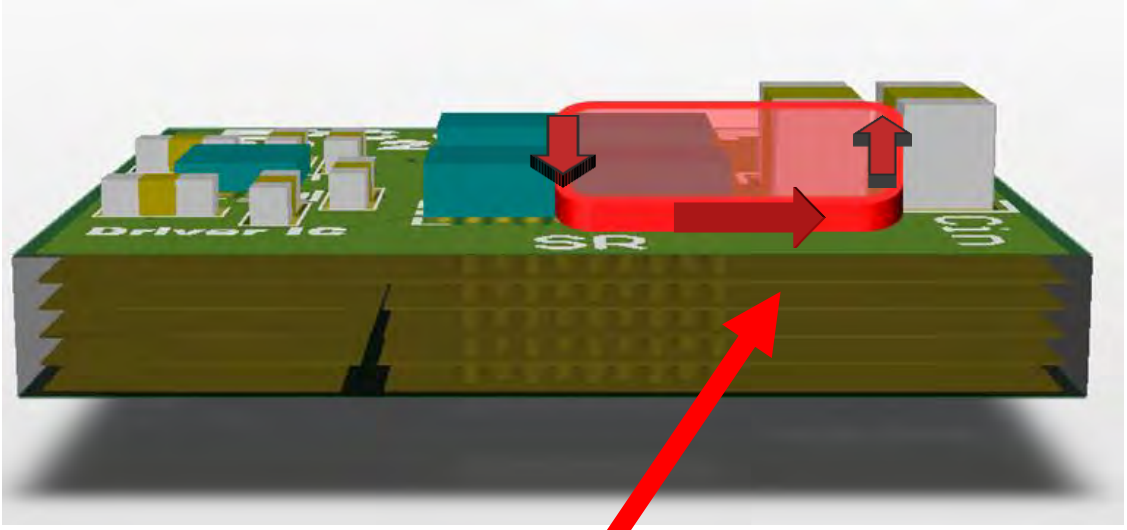
# Conventional Lateral Layout



## Top View



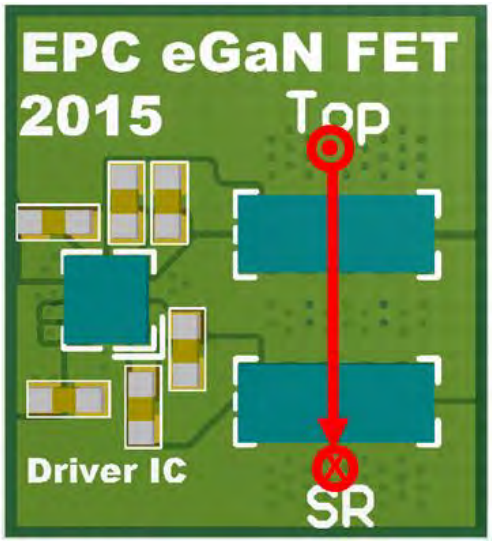

## Side View




**Shield Layer**

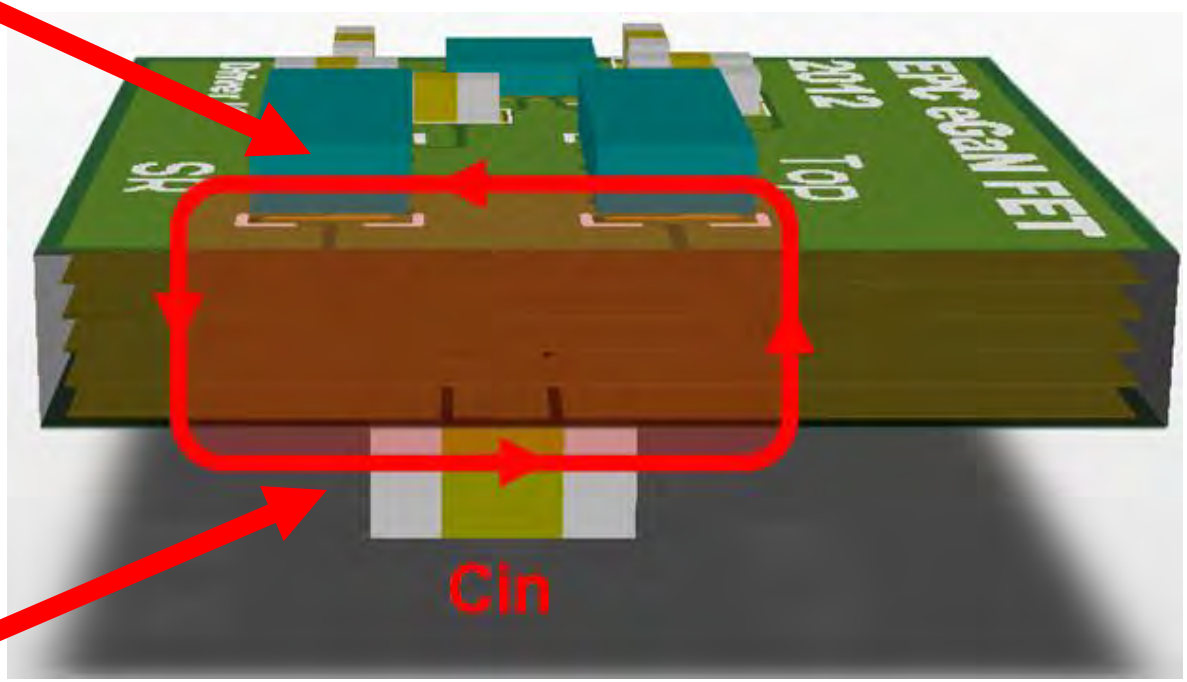
# Conventional Vertical Layout

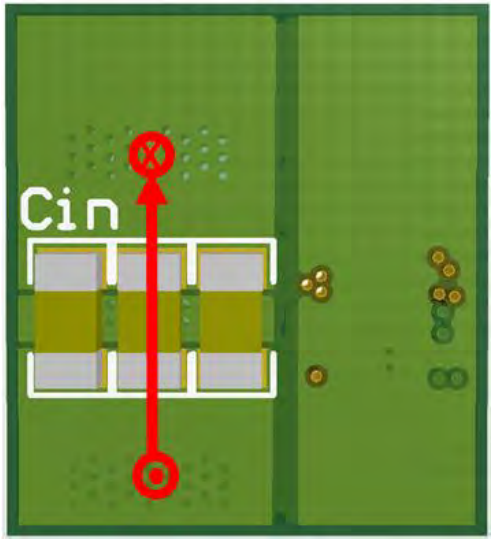





Top View

Side View

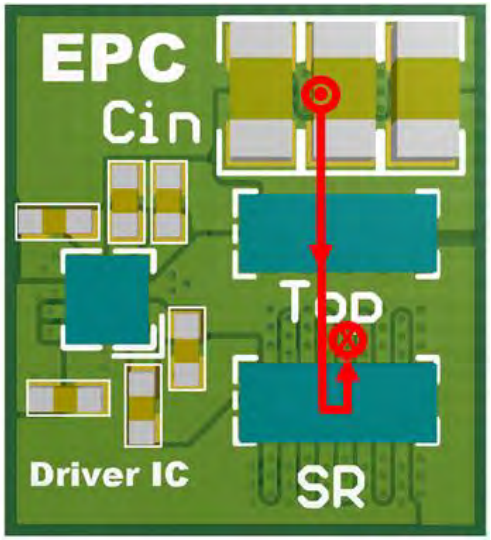



Bottom View

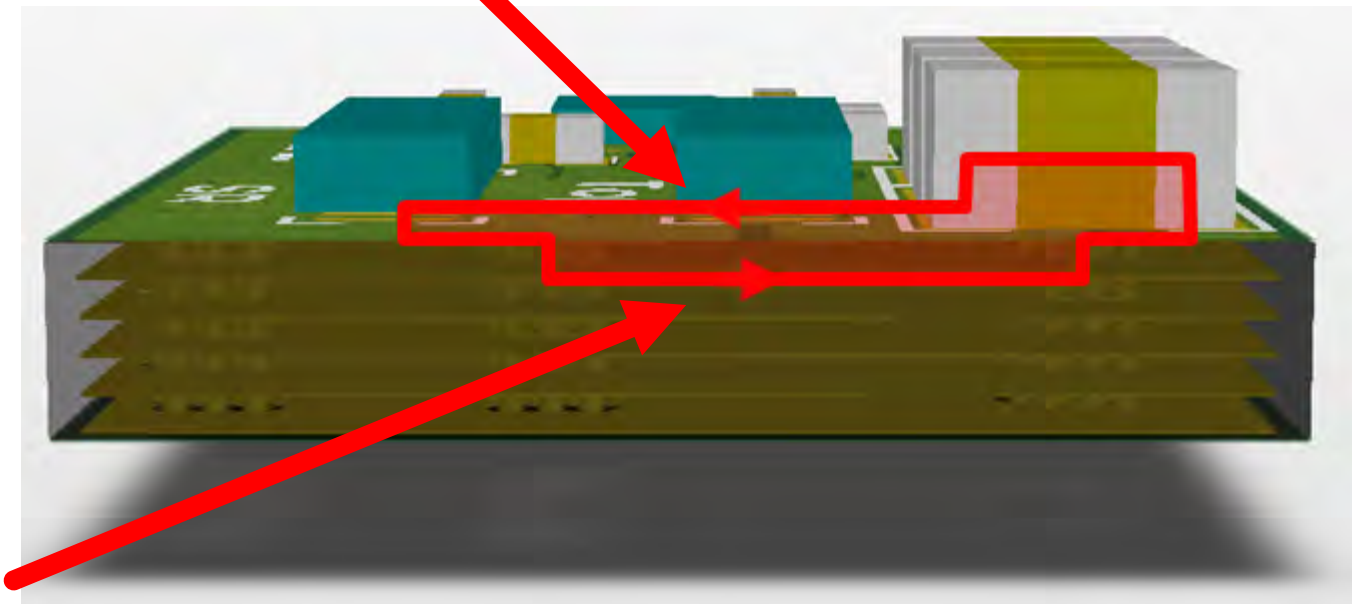
# EPC Optimal Layout

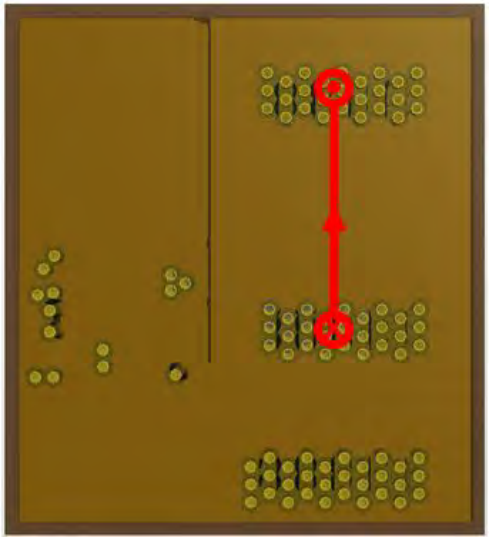





Top View

Side View

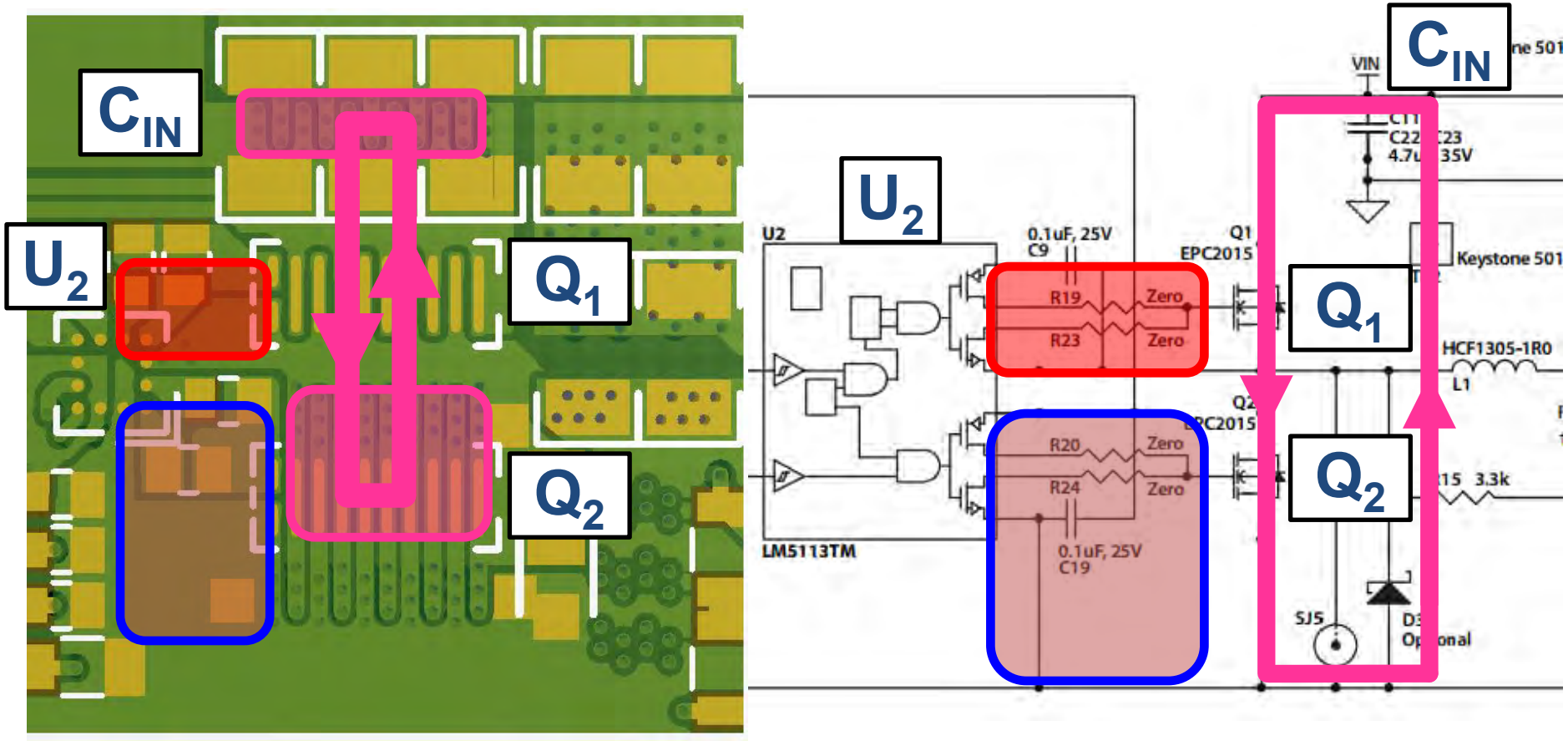




Top View
Inner Layer 1

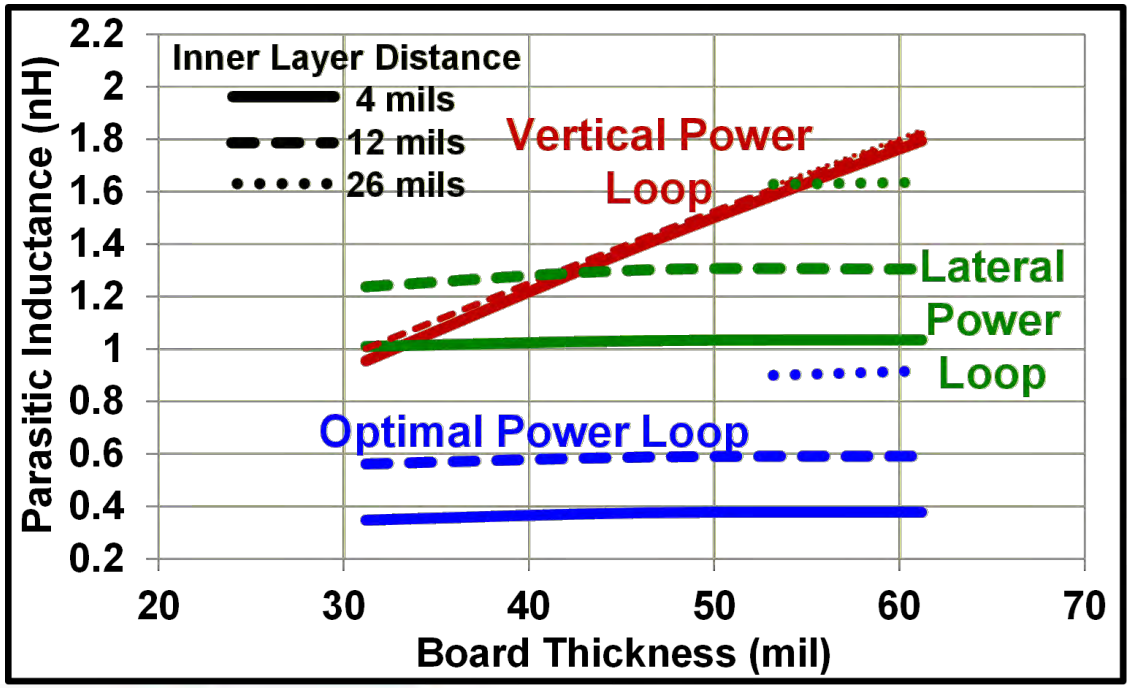
# Optimal Layout Implementation

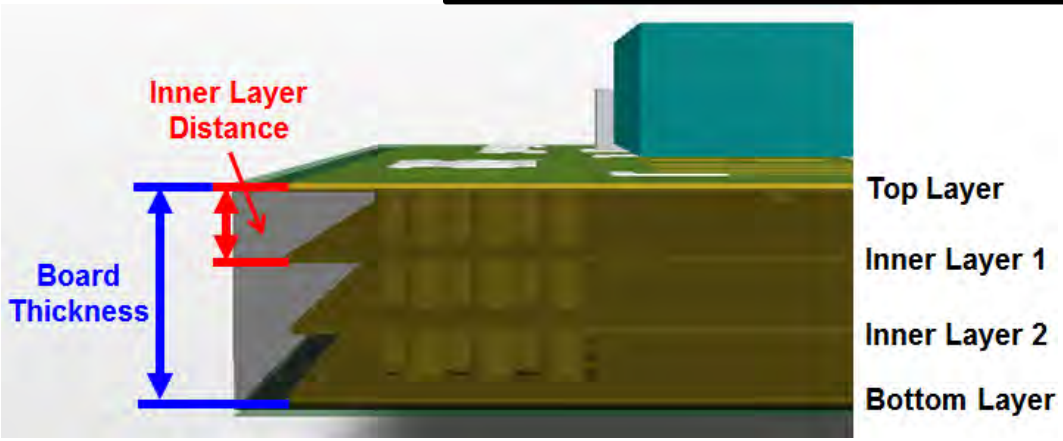




# Layout Inductance Comparison





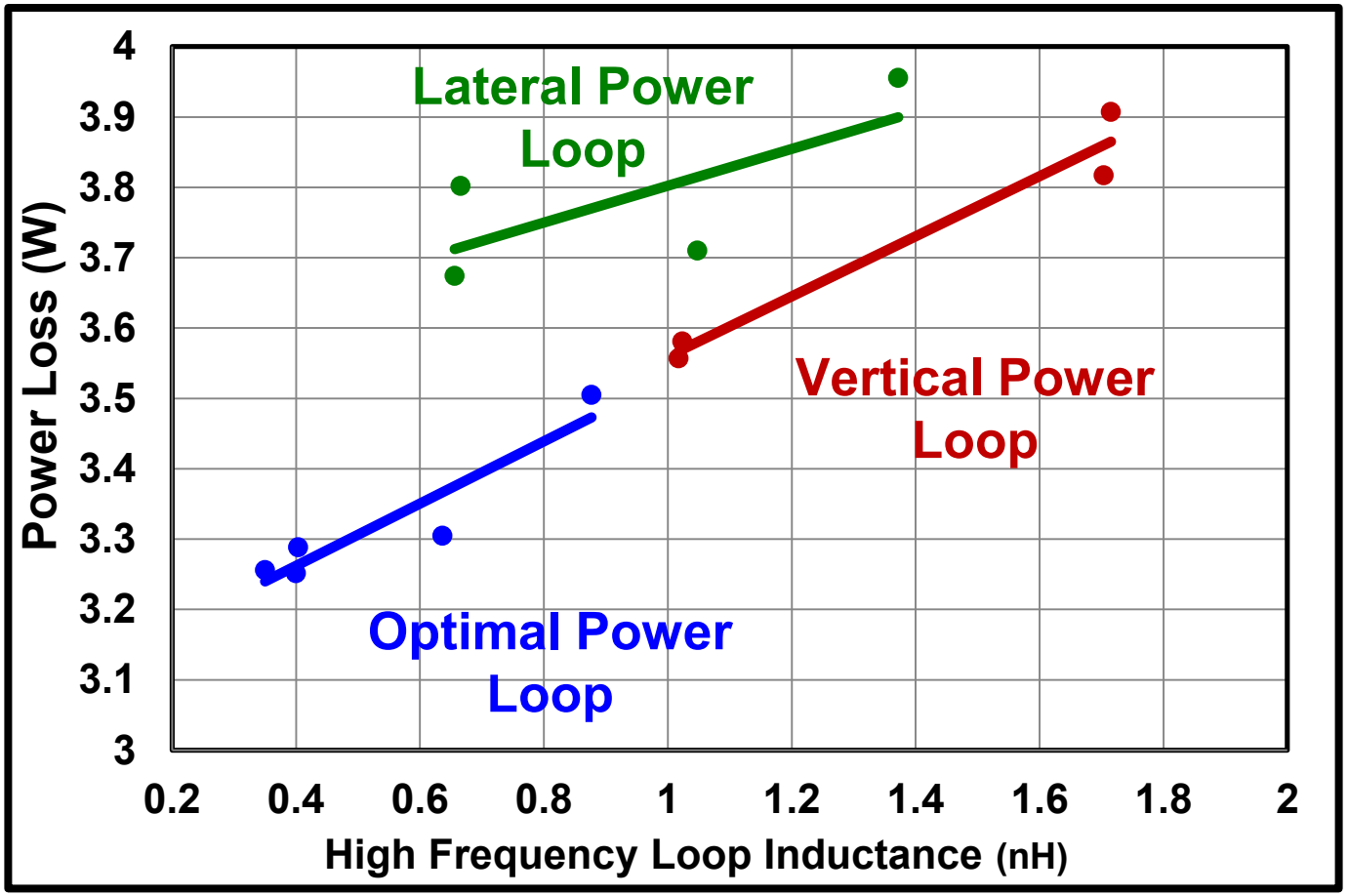




## Test Cases

| | Board Thickness (mils) | Inner Layer Distance (mils) |
|---|---|---|
| Design 1 | 31 | 4 |
| Design 2 | 31 | 12 |
| Design 3 | 62 | 4 |
| Design 4 | 62 | 26 |

# Power Loss Comparison

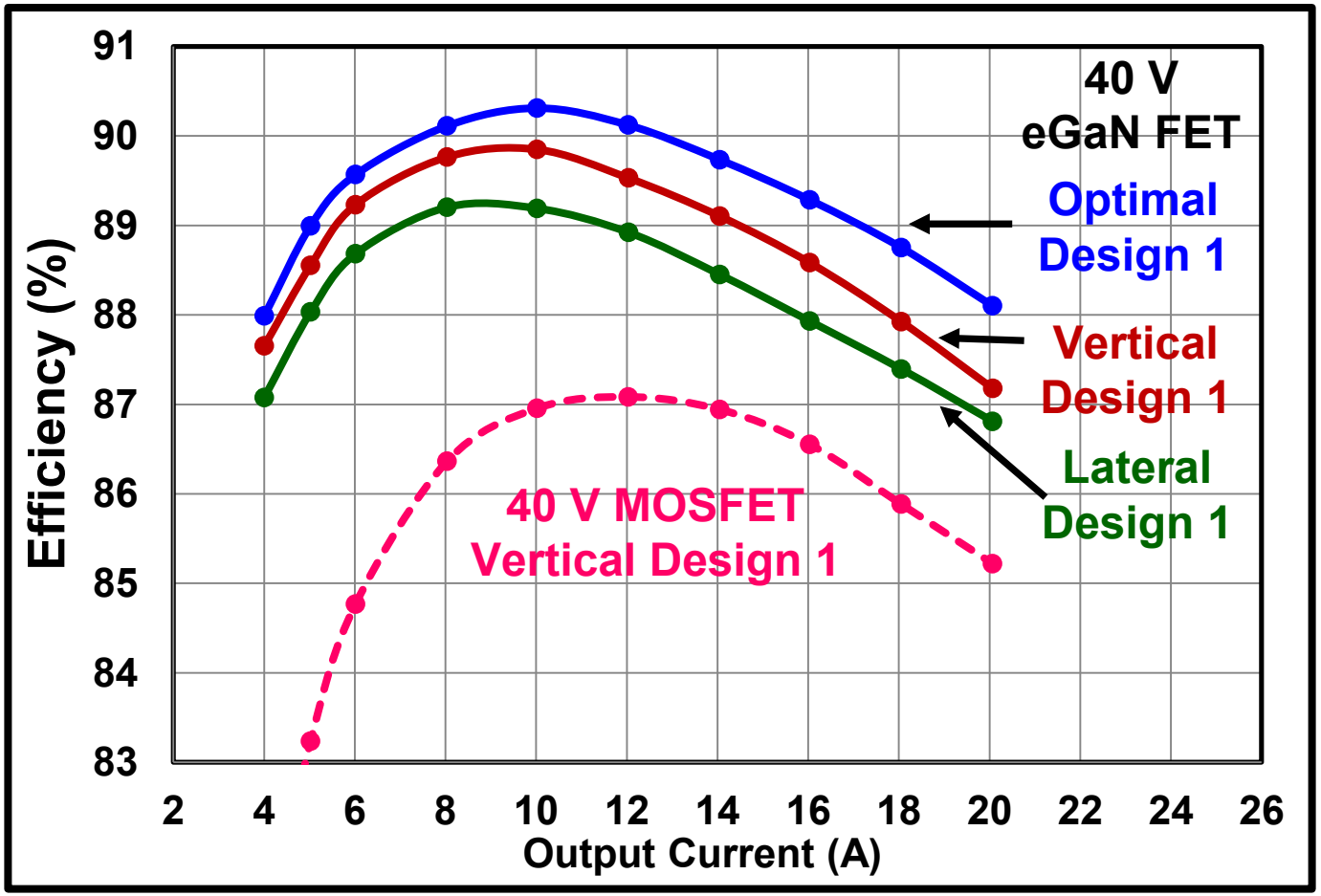





**$V_{IN}$=12 V $V_{OUT}$=1.2 V $I_{OUT}$=20 A $f_{sw}$=1 MHz L=300 nH**
**T/SR: EPC2015 Driver LM5113**

# Efficiency Comparison



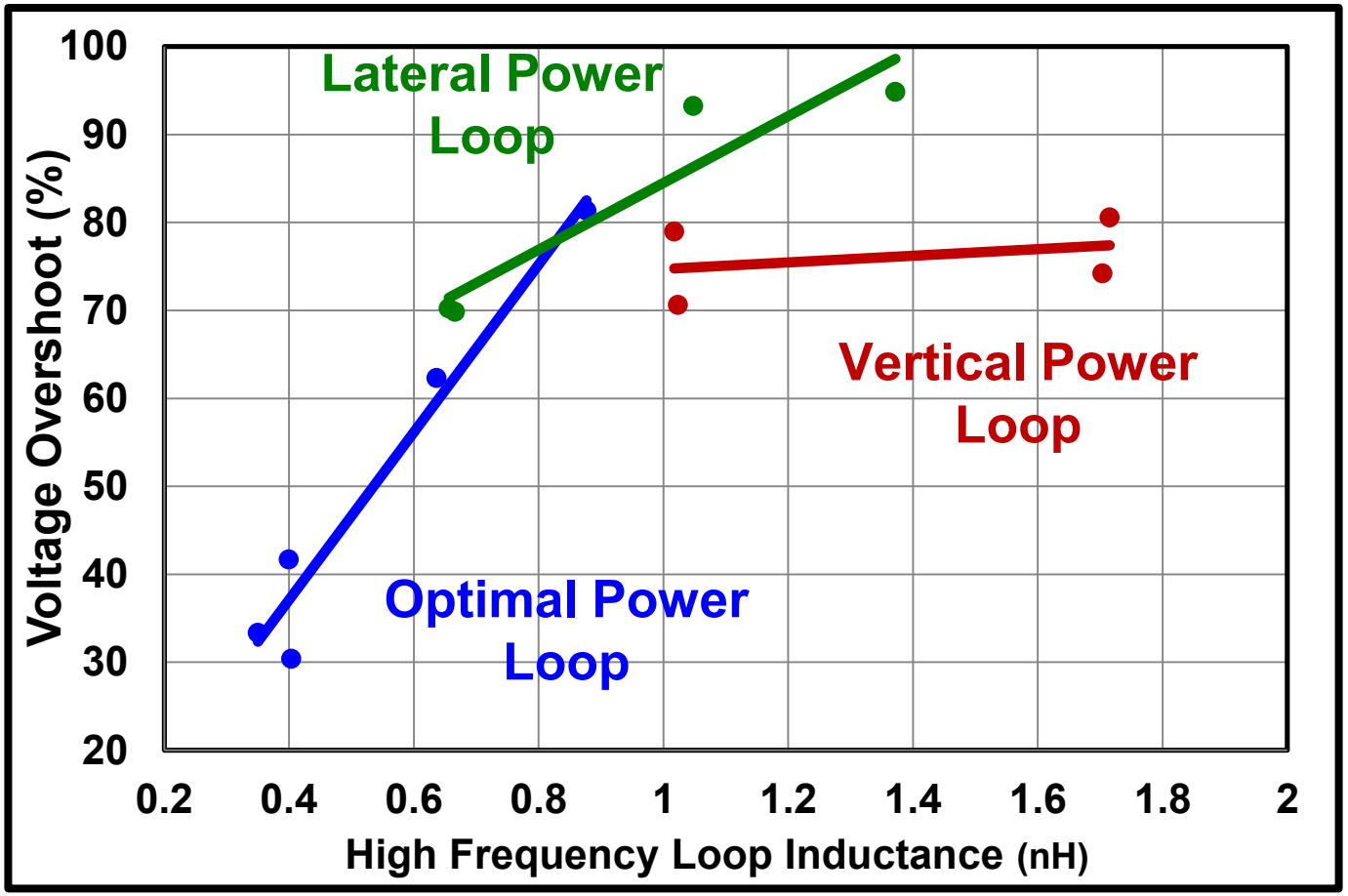



**$V_{IN}$=12 V $V_{OUT}$=1.2 V $f_{sw}$=1 MHz L=300 nH**

**GaN T/SR: EPC2015 Driver LM5113**

# Voltage Overshoot Comparison

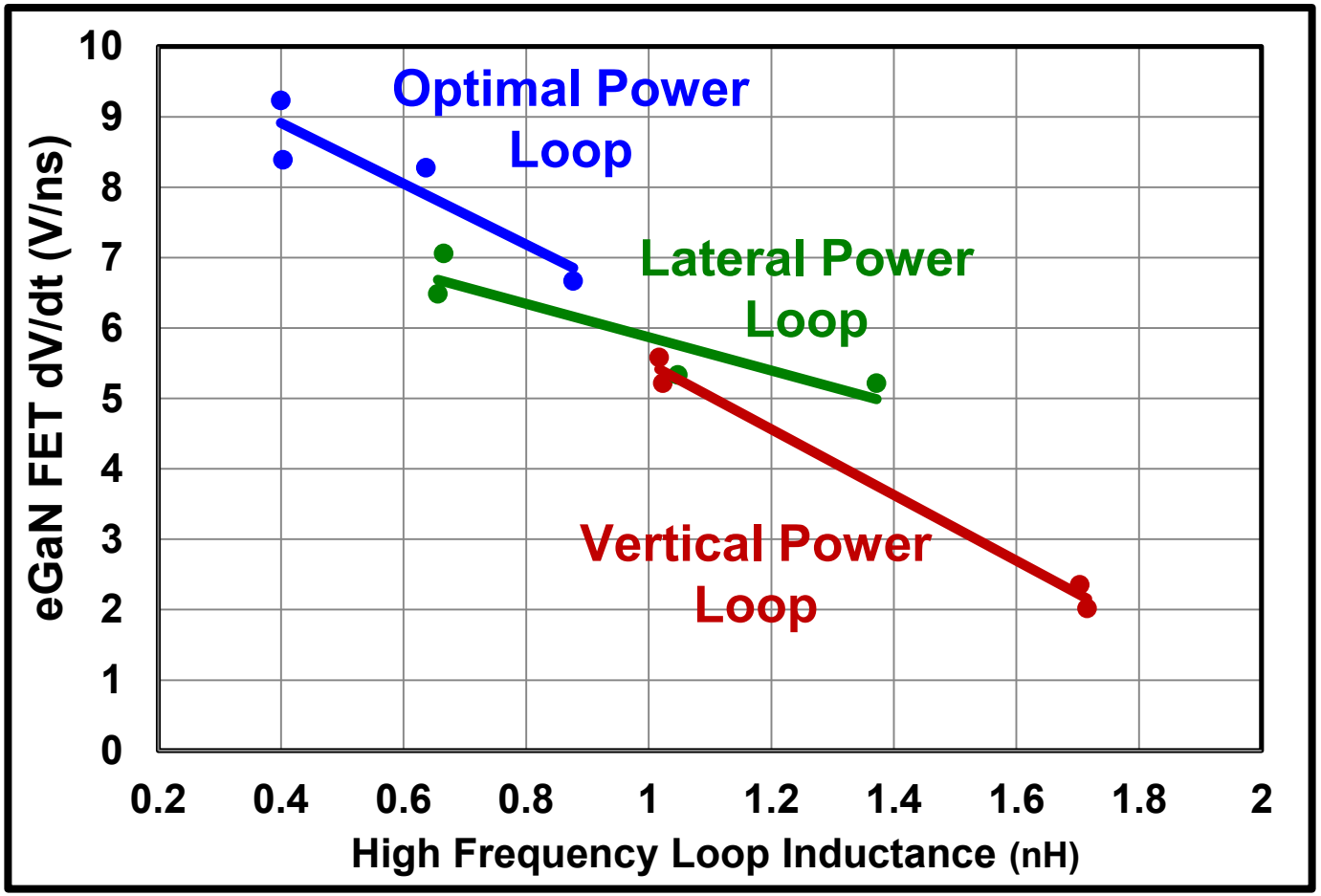





$V_{IN}$=12 V $V_{OUT}$=1.2 V $I_{OUT}$=20 A $f_{sw}$=1 MHz L=300 nH
T/SR: EPC2015 Driver LM5113

# Switching Speed Comparison



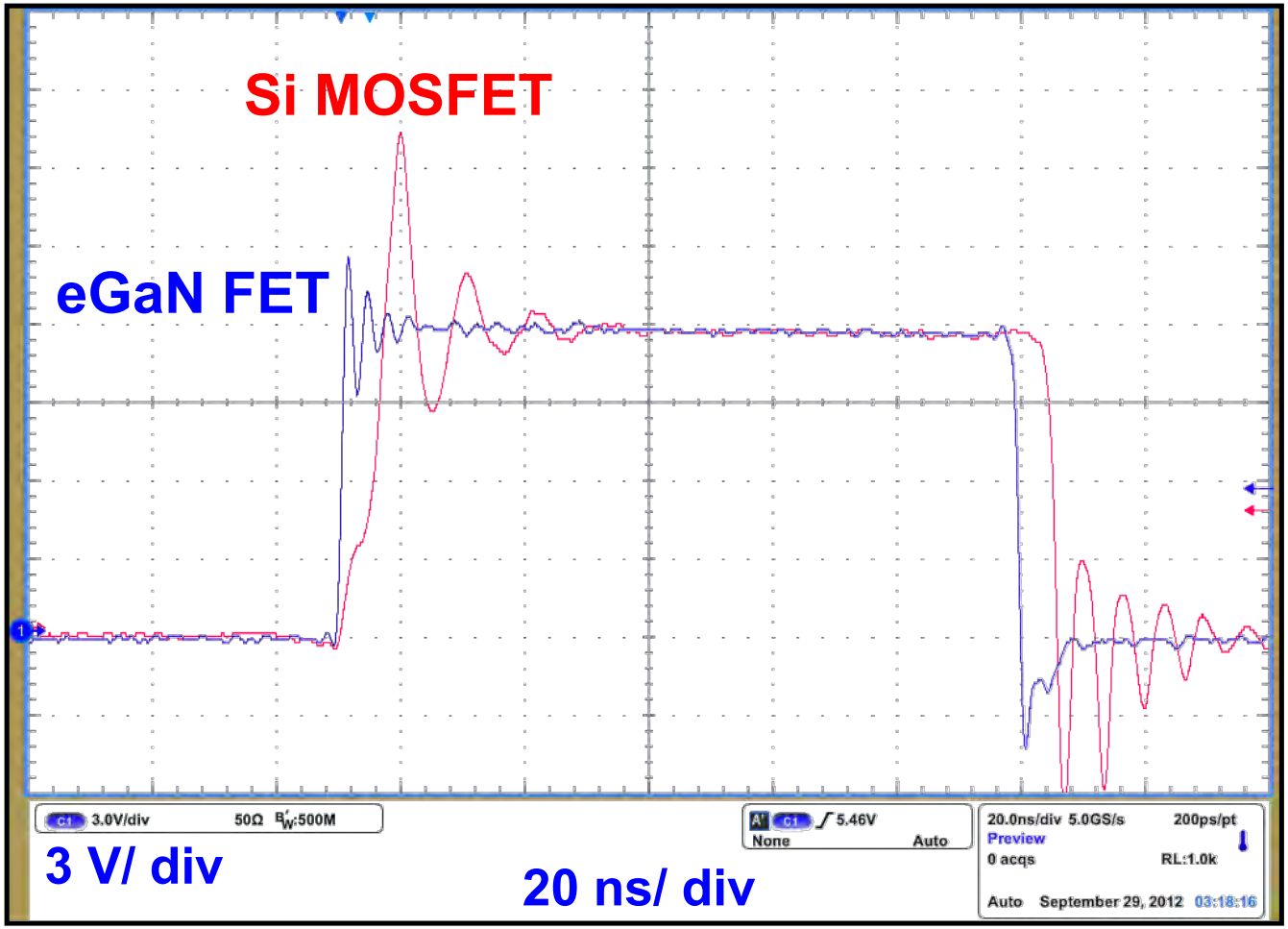



$V_{IN}$=12 V $V_{OUT}$=1.2 V $I_{OUT}$=20 A $f_{sw}$=1 MHz L=300 nH

T/SR: EPC2015 Driver LM5113

# eGaN FET vs. MOSFET



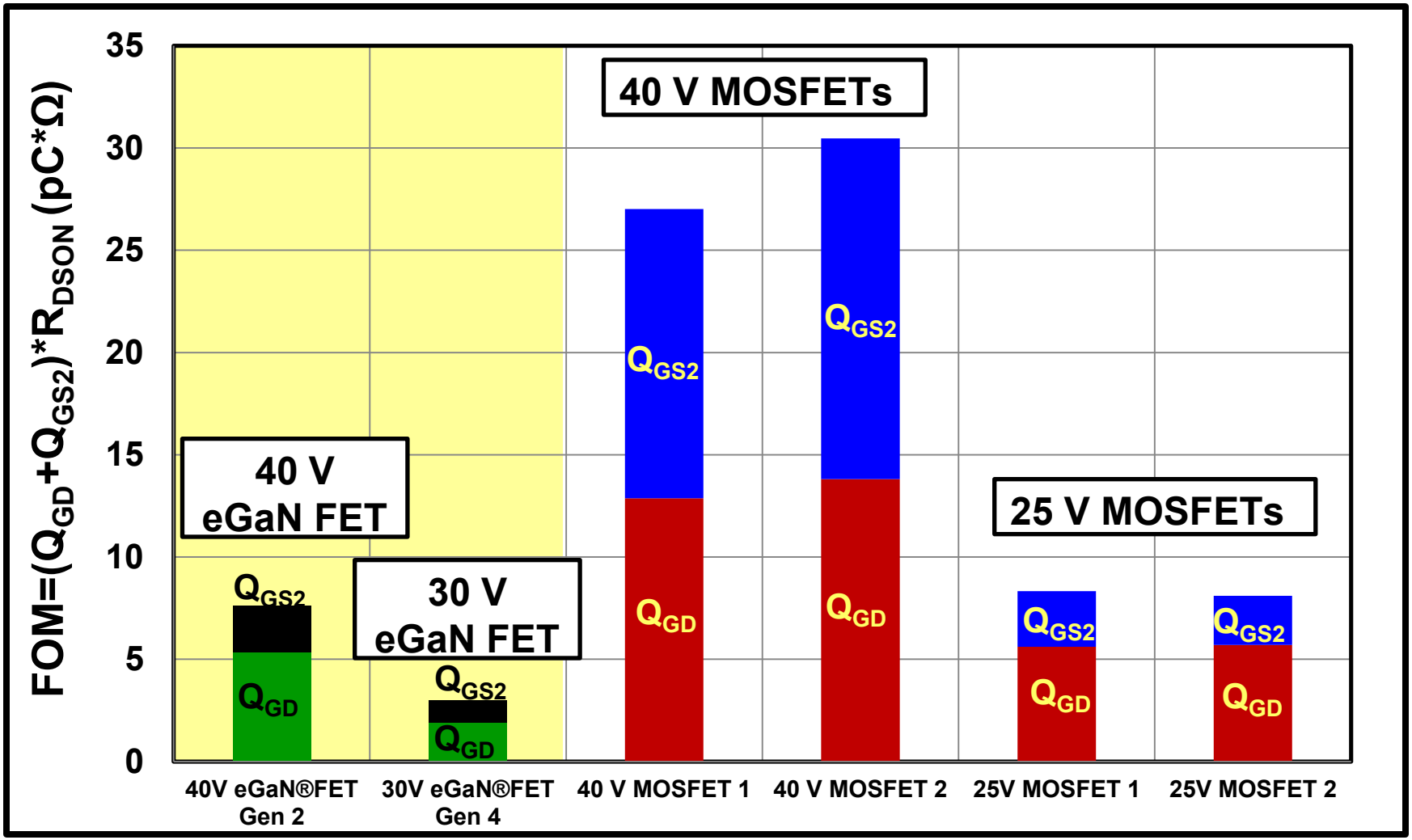



$V_{IN}$=12 V $V_{OUT}$=1.2 V $I_{OUT}$=20 A $f_{sw}$=1 MHz L=300 nH eGaN FET

T/SR: EPC2015 MOSFET T:BSZ097N04 SR:BSZ040N04

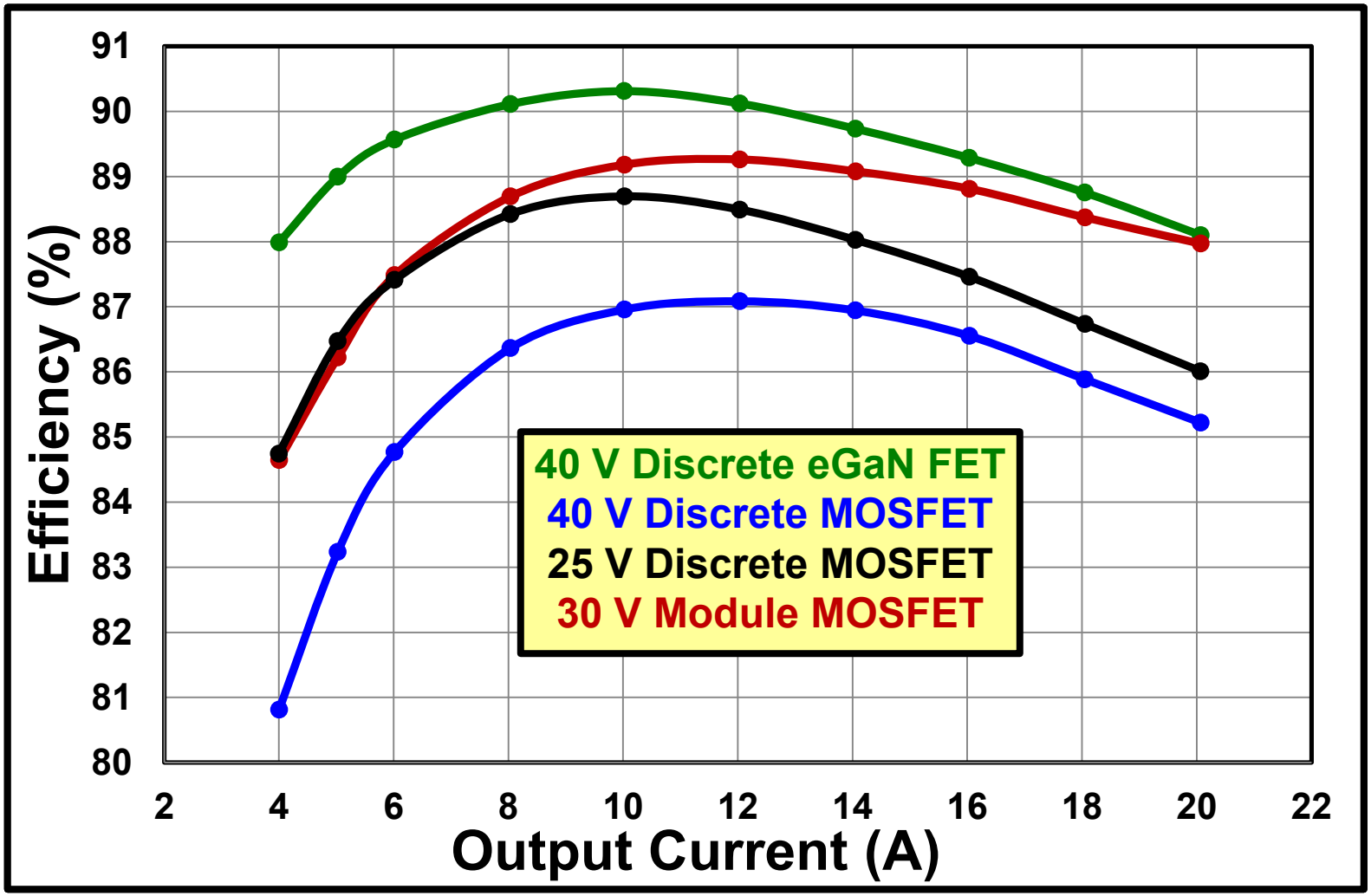
# Lower Voltage Comparison





# Lower Voltage Comparison

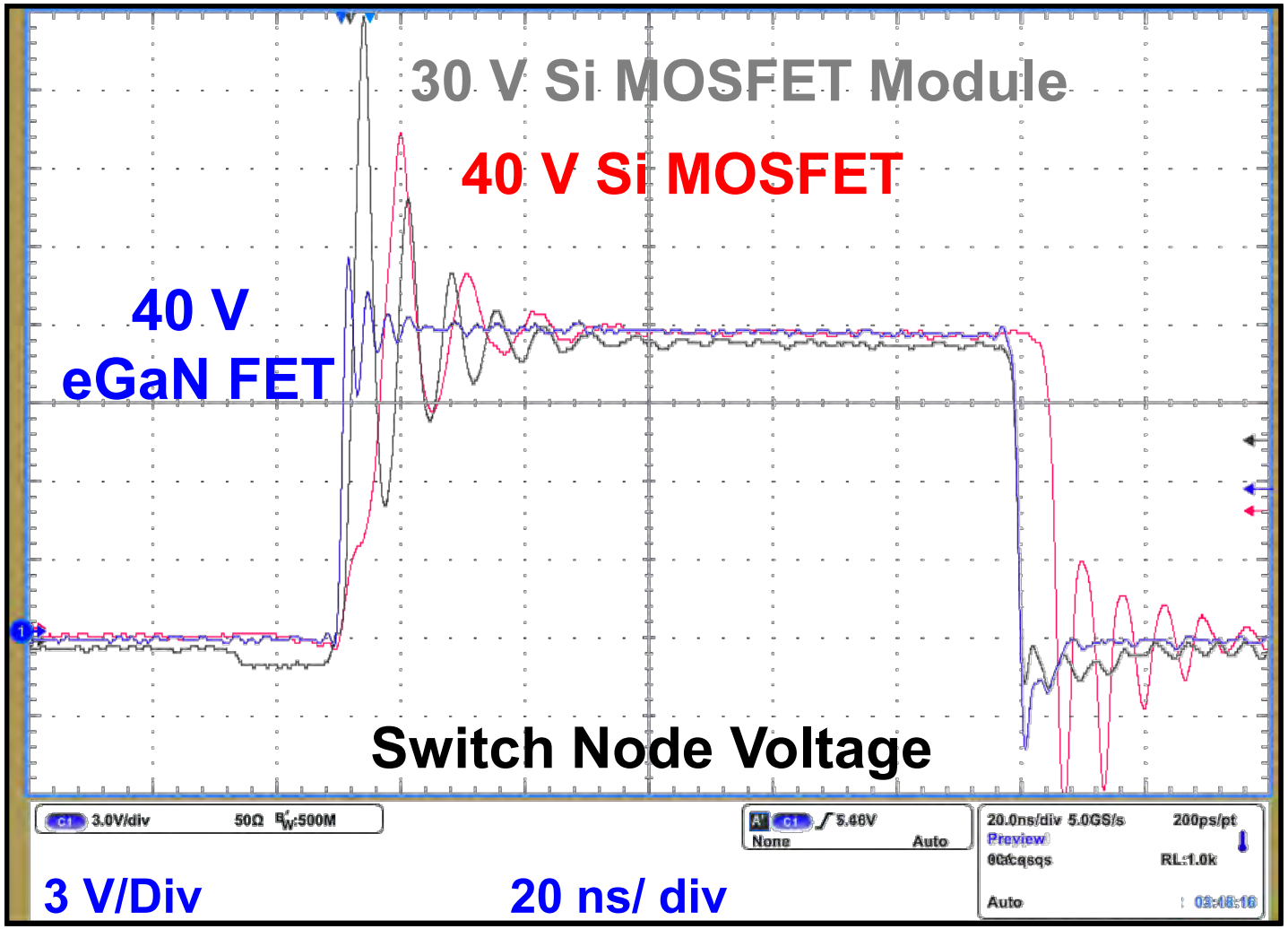





$V_{IN}$=12 V $V_{OUT}$=1.2 V $f_{sw}$=1 MHz L=300 nH

# Switching Comparison

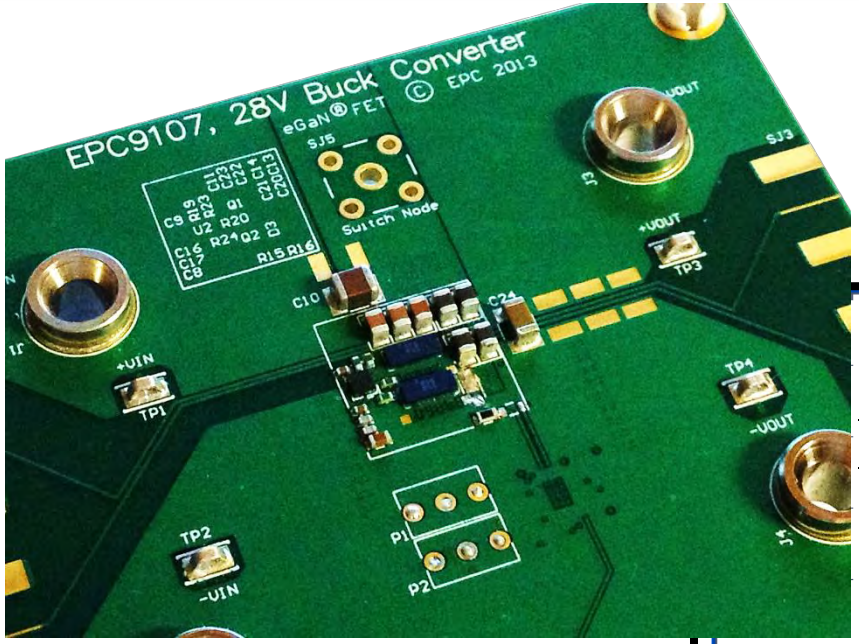




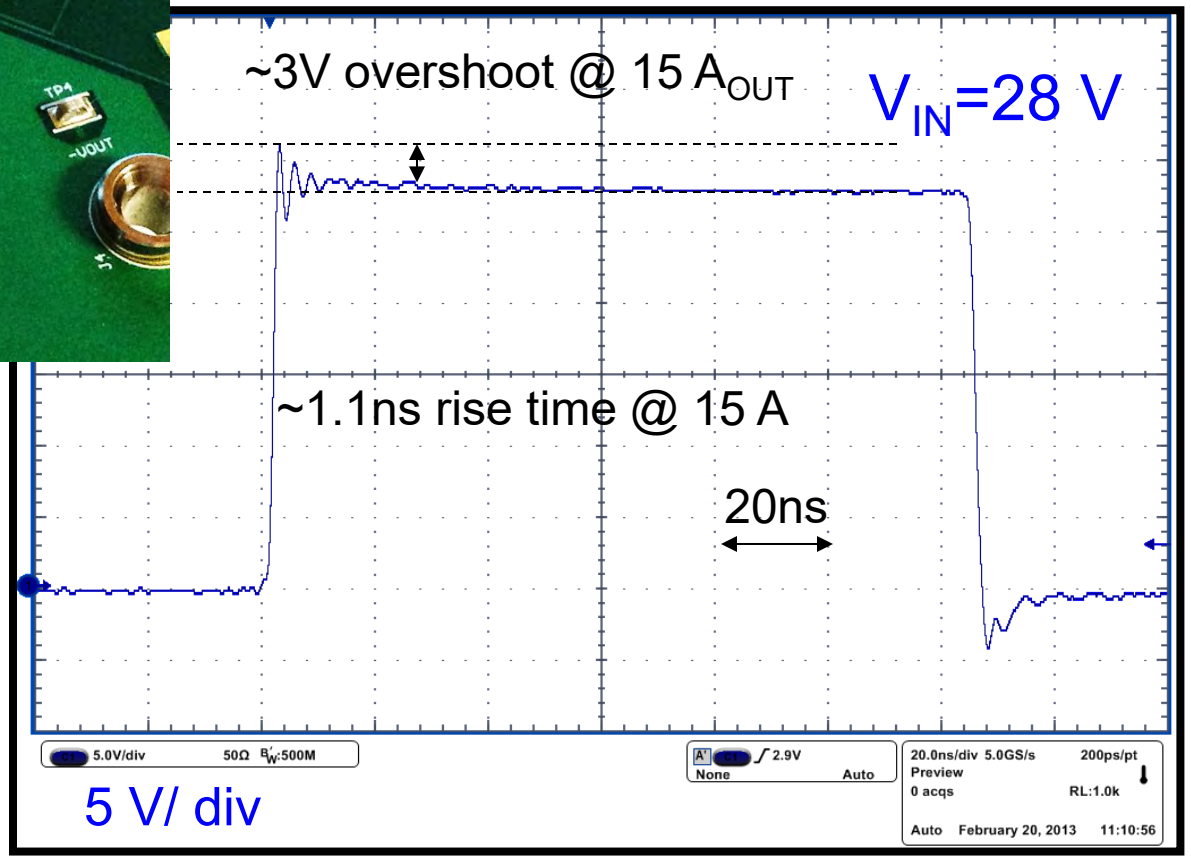

$V_{IN}$=12 V $V_{OUT}$=1.2 V $I_{OUT}$=20 A $f_{sw}$=1 MHz L=300 nH

# EPC9107 Demonstration Board






$V_{IN}$=12-28 V $V_{OUT}$=3.3 V
$I_{OUT}$=15 A $f_{sw}$=1 MHz
2 x EPC2015

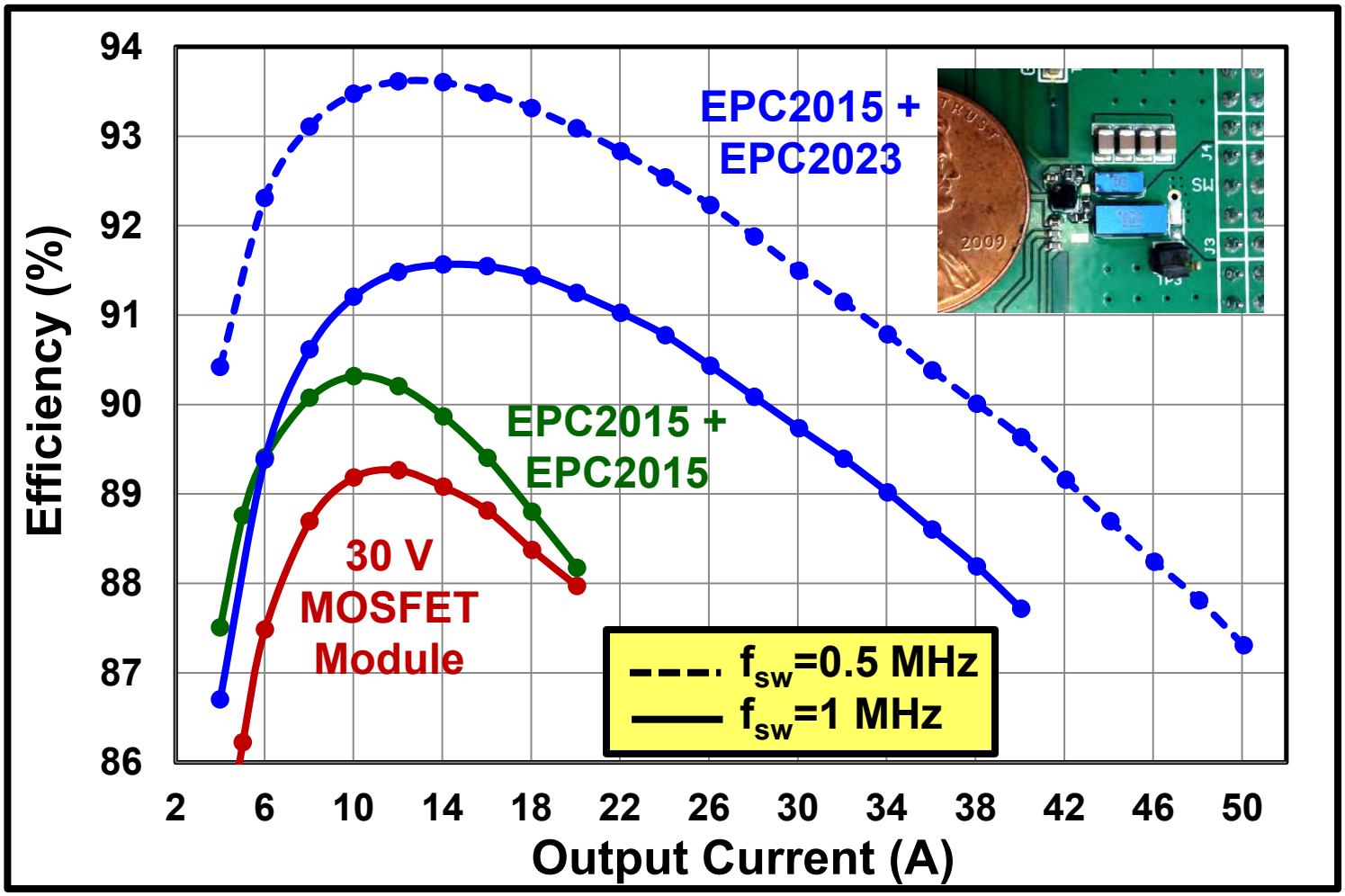



## Switching Node Voltage

$V_{IN}$=28 V, $I_{OUT}$=15 A

# Higher Current Devices

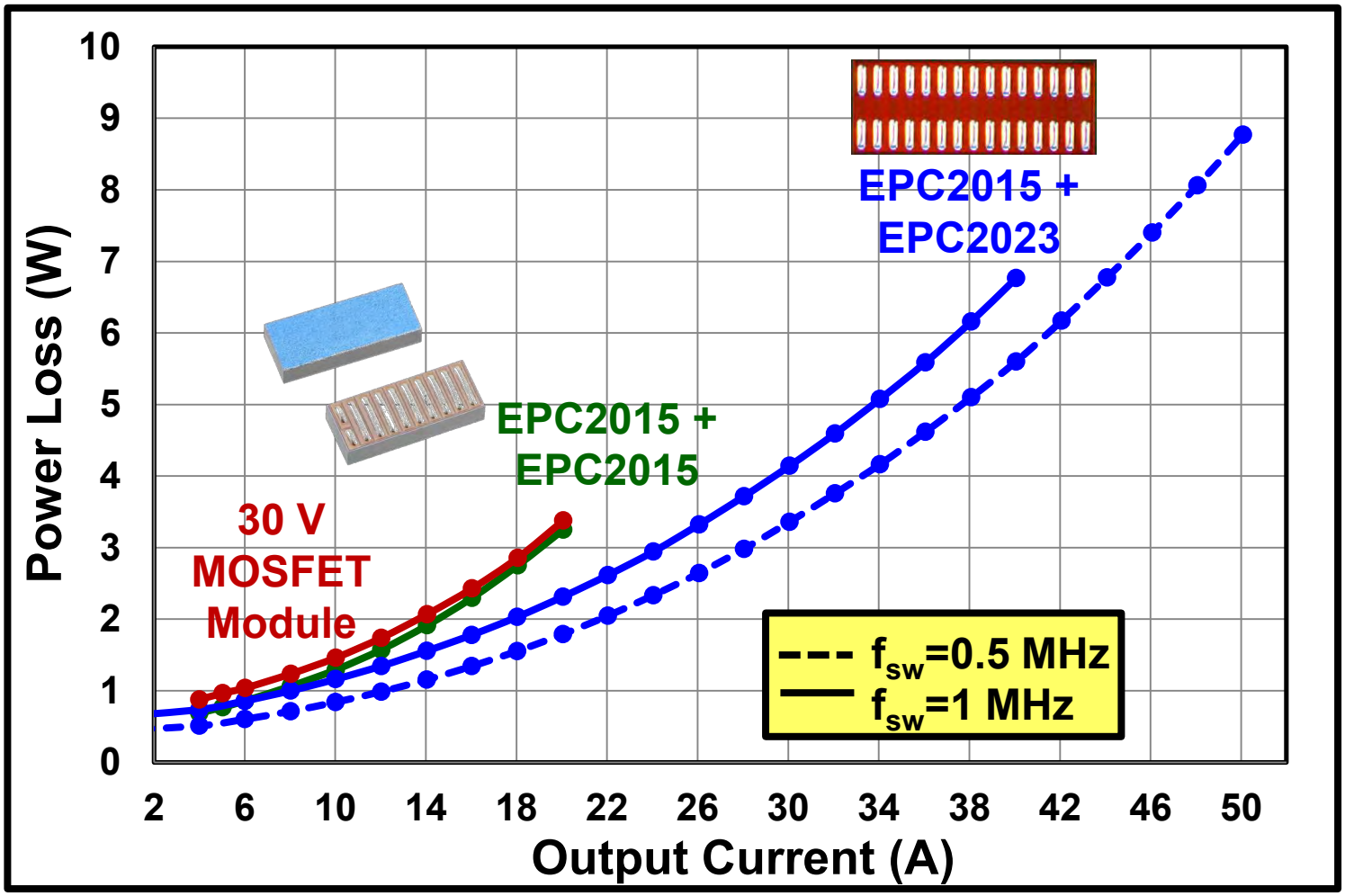





$V_{IN}$=12 V $V_{OUT}$=1.2 V

# Higher Current Devices



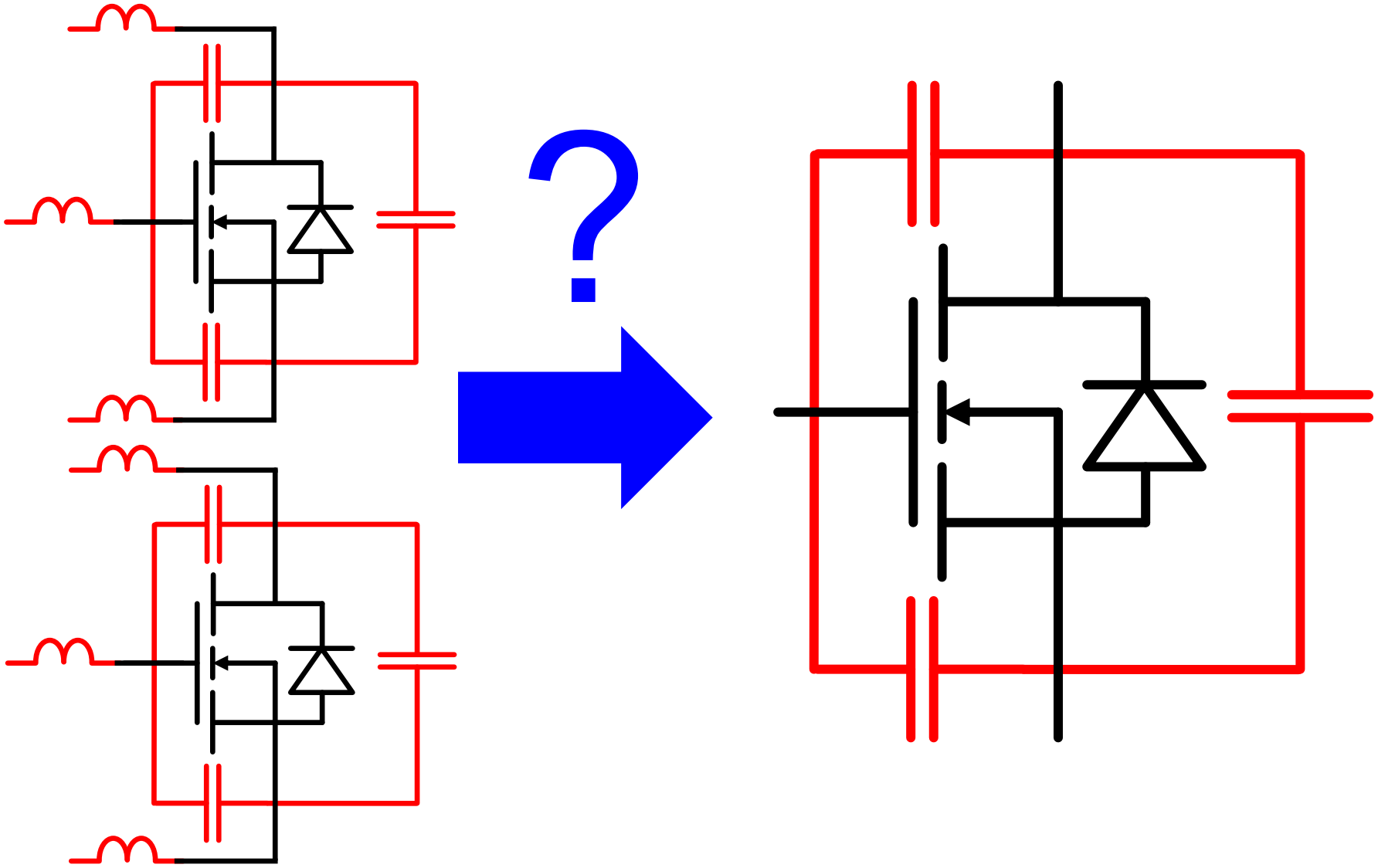



$V_{IN}$=12 V $V_{OUT}$=1.2 V

# Paralleling High-Speed eGaN FETs

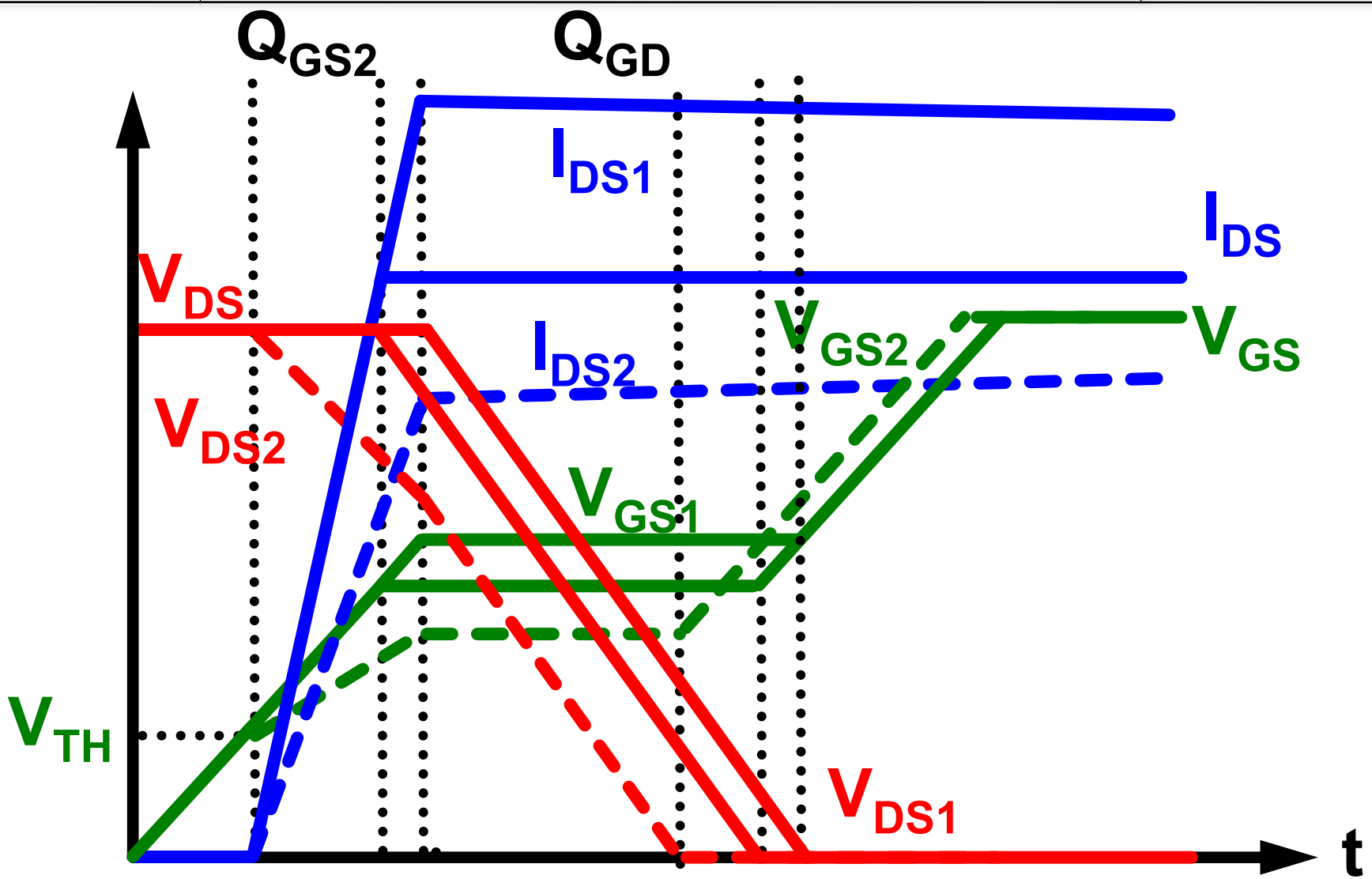
# Parallel Power Devices





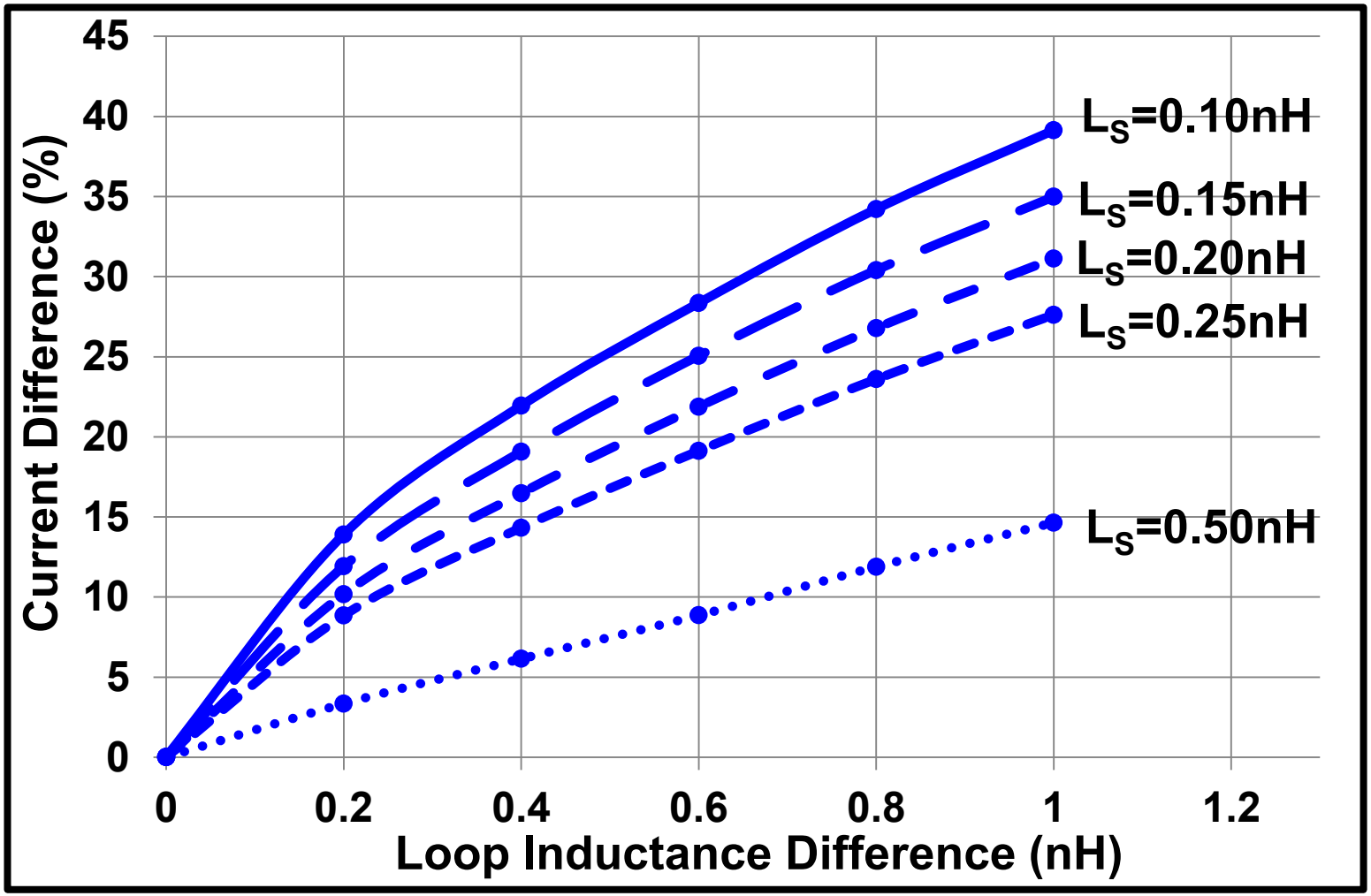
# Unbalanced Loop Inductance





# Loop Inductance Impact

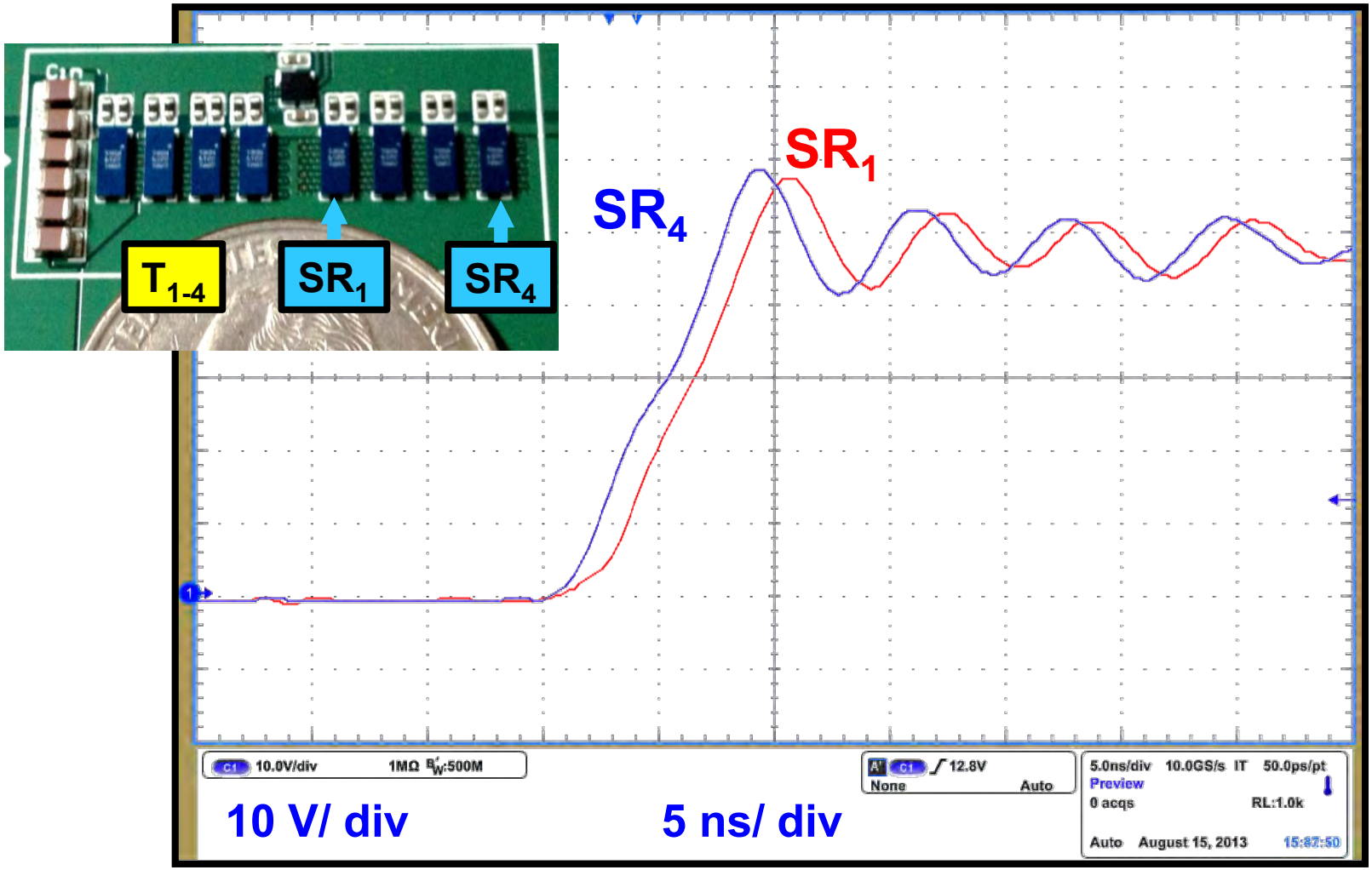





$V_{IN}$=48 V $I_{OUT}$=25 A eGaN FET T/SR: 100 V EPC2001

# Single Loop Optimal Layout

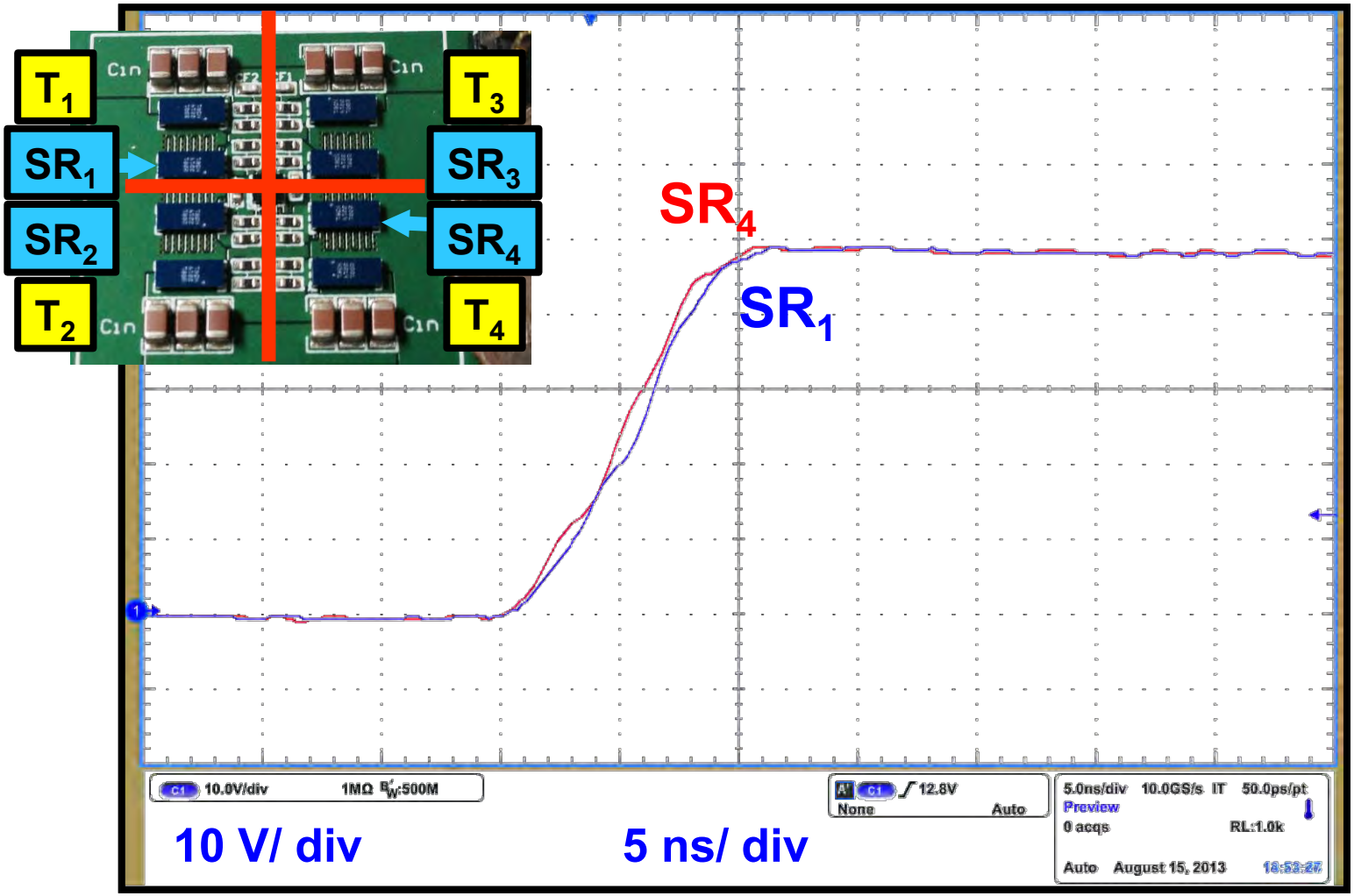





$V_{IN}$=48 V $V_{OUT}$=12 V $I_{OUT}$=30 A $f_{sw}$=300 kHz L=3.3 µH GaN FET T/SR: 100 V EPC2001

# Parallel Loop Optimal Layout

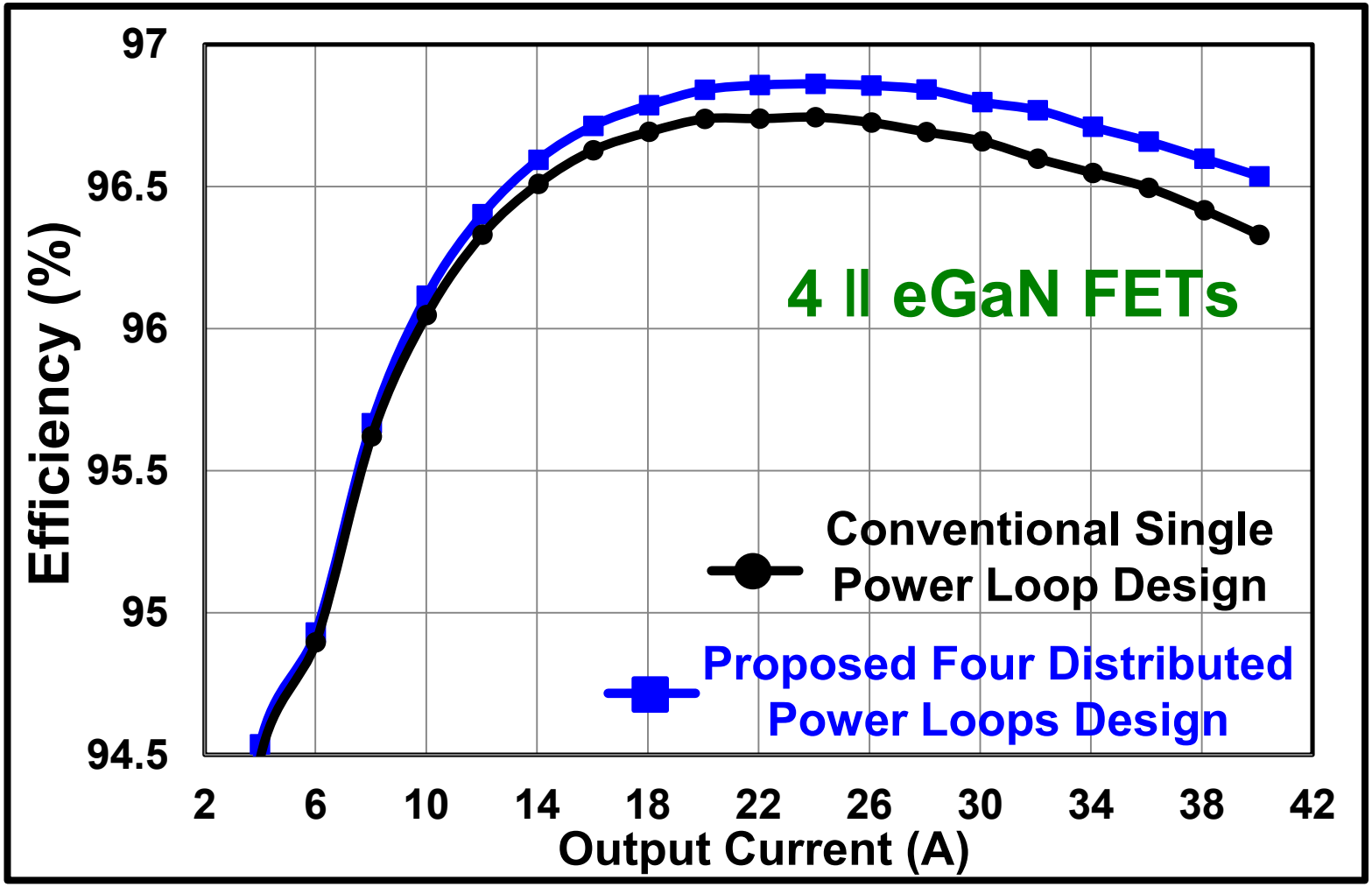





$V_{IN}$=48 V $V_{OUT}$=12 V $I_{OUT}$=30 A $f_{sw}$=300 kHz L=3.3 µH GaN FET T/SR: 100 V EPC2001

# Parallel Layout Performance

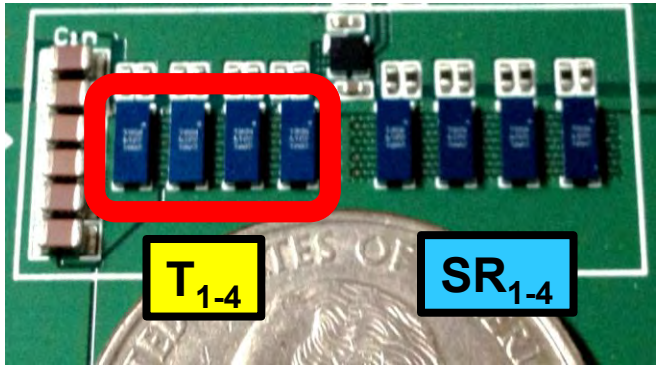


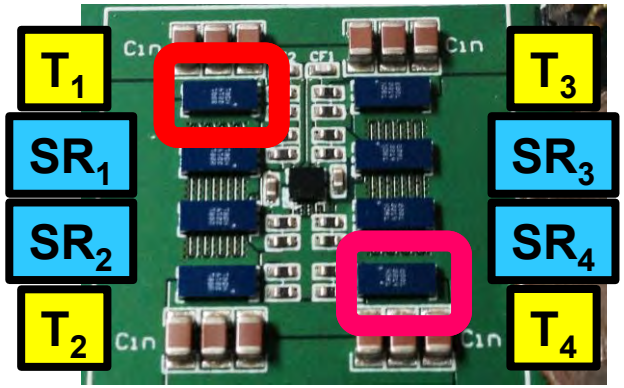


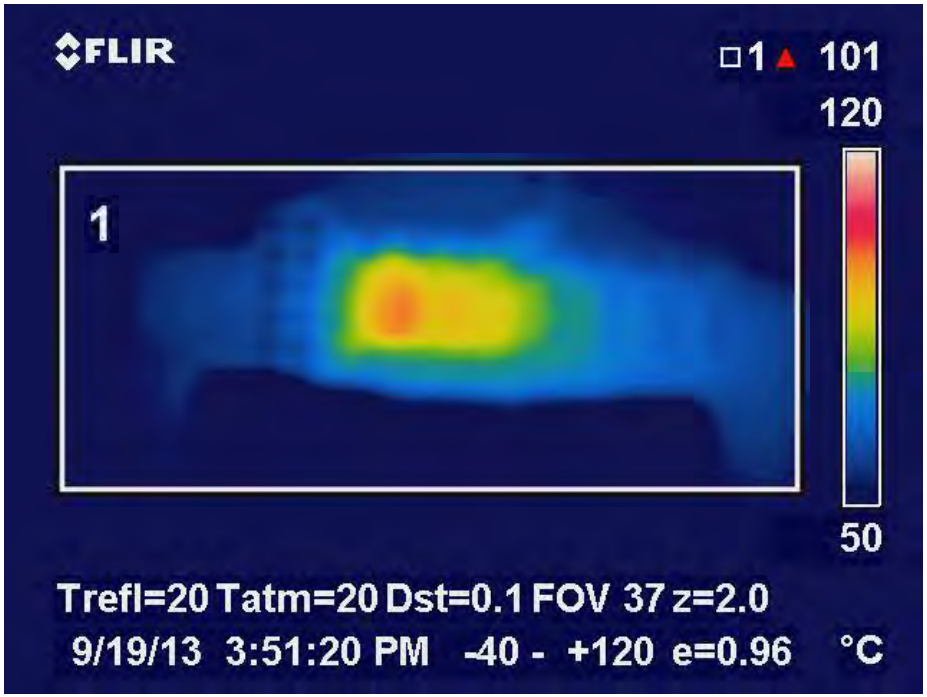

$V_{IN}$=48 V $V_{OUT}$=12 V $f_{sw}$=300 kHz L=3.3 µH GaN FET T/SR: 4x100 V EPC2001
4 Layer 2 oz PCB

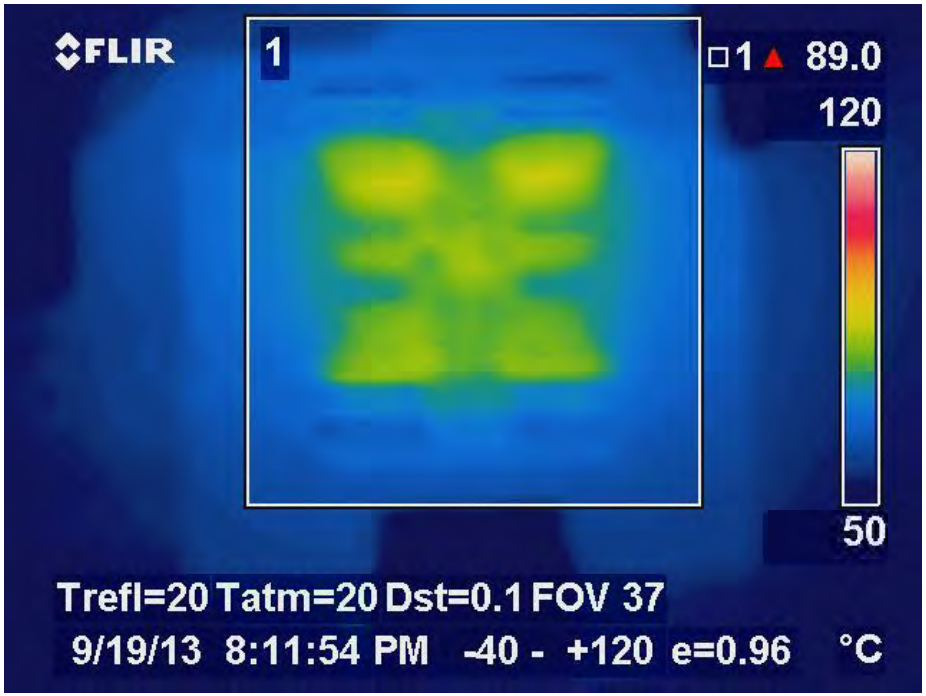
# Parallel Layout Implementation





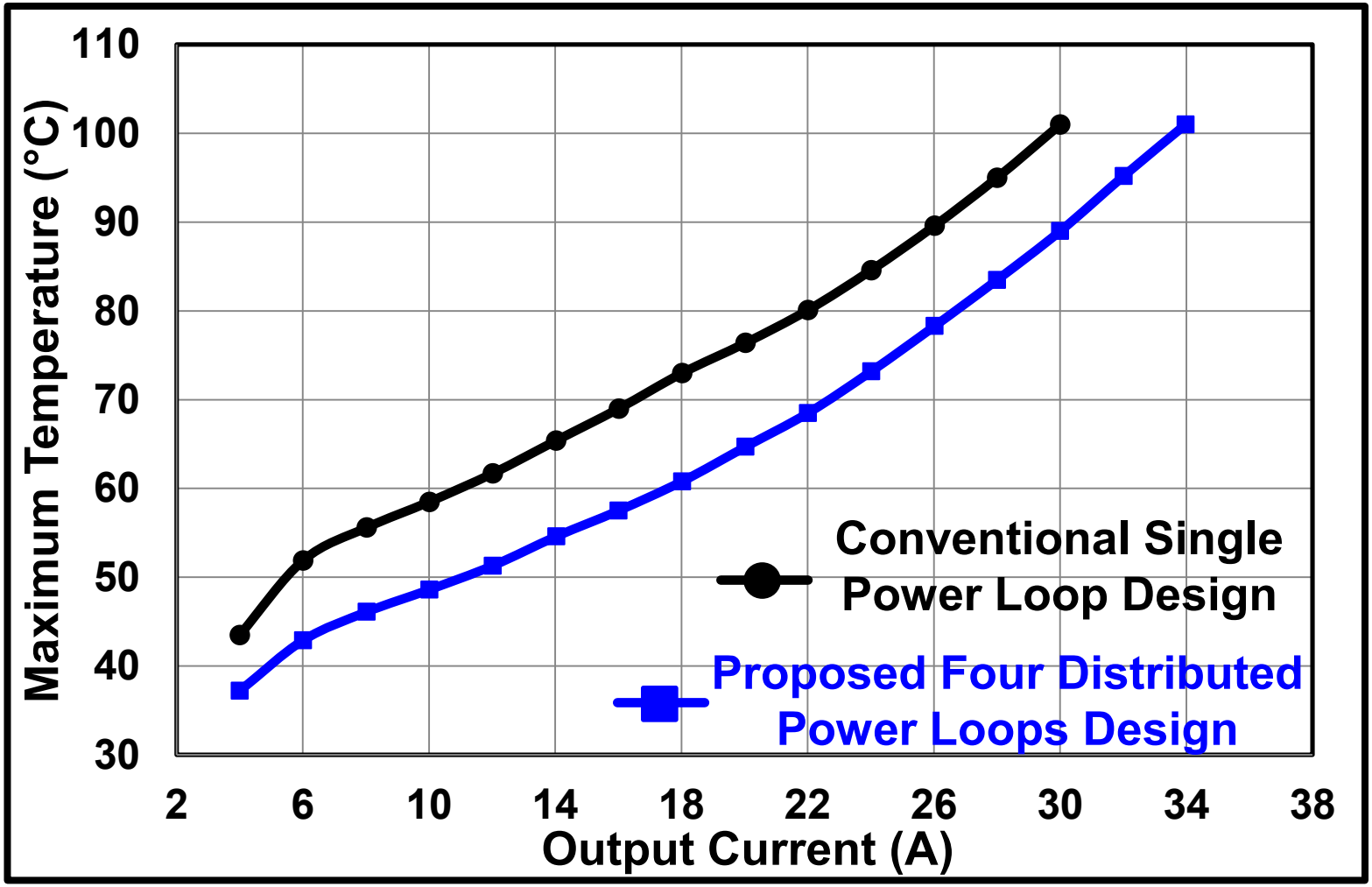




$V_{IN}$=48 V $V_{OUT}$=12 V $I_{OUT}$=30 A $f_{sw}$=300 kHz L=3.3 µH GaN FET T/SR: 100 V EPC2001

# Parallel Layout Performance

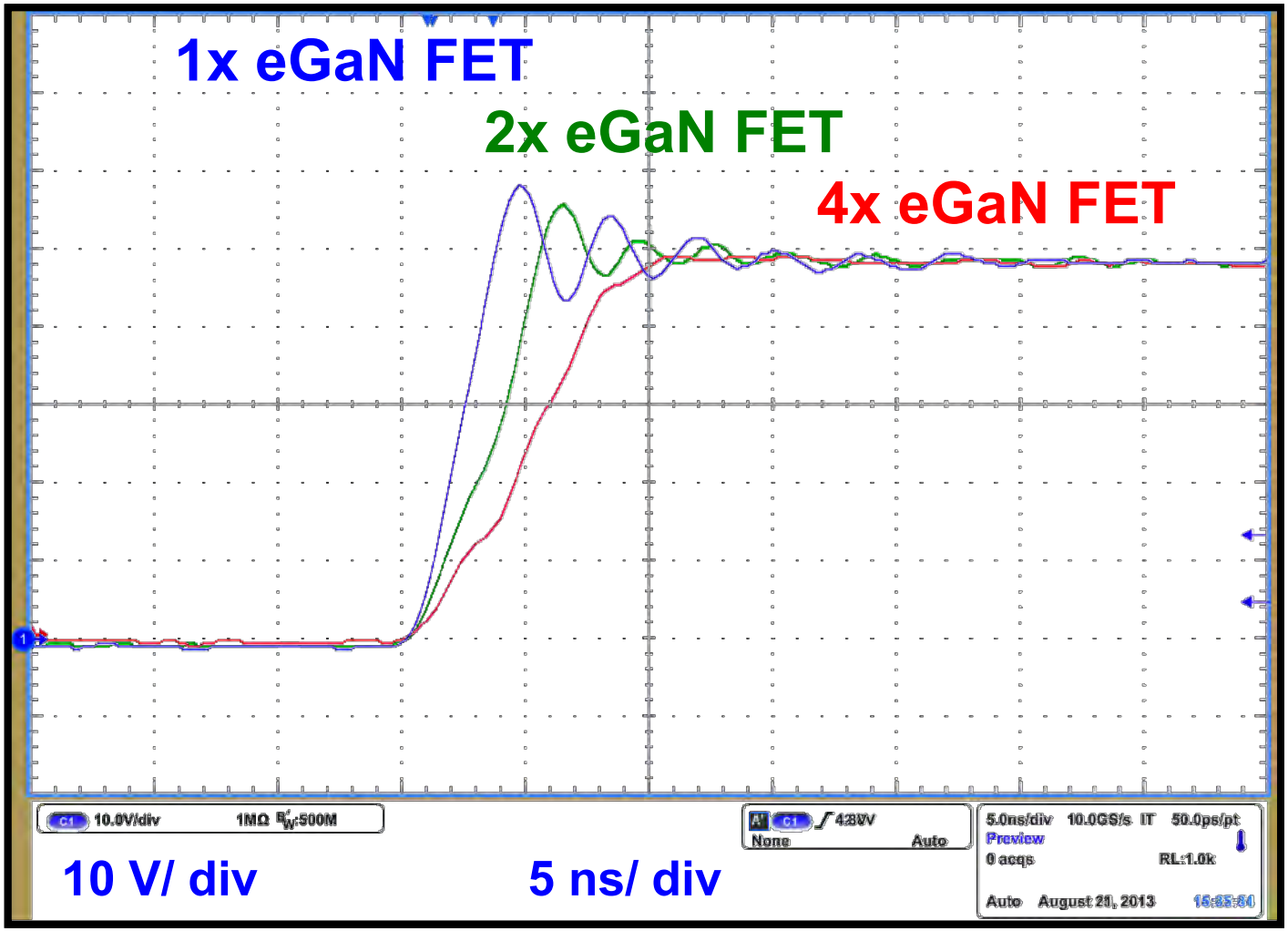





$V_{IN}$=48 V $V_{OUT}$=12 V $f_{sw}$=300 kHz L=3.3 µH GaN FET T/SR: 100 V EPC2001
Fan Speed 200 LFM 4 Layer 2 oz PCB

# Parallel eGaN FET Switching

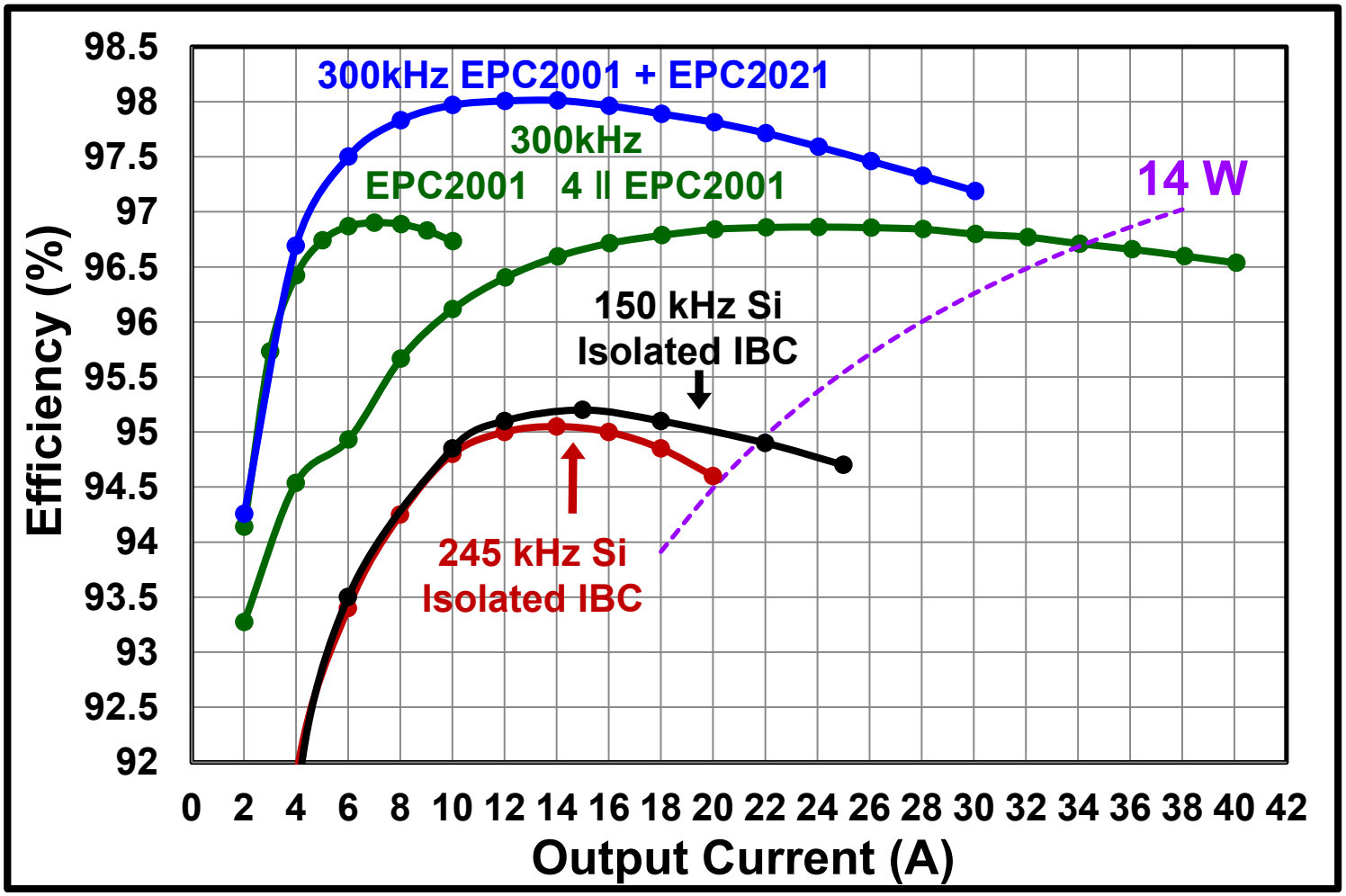





$V_{IN}$=48 V $V_{OUT}$=12 V $I_{OUT}$=30 A/ number of devices $f_{sw}$=300 kHz GaN FET T/SR: 100 V EPC2001

# Parallel Buck in IBC Applications

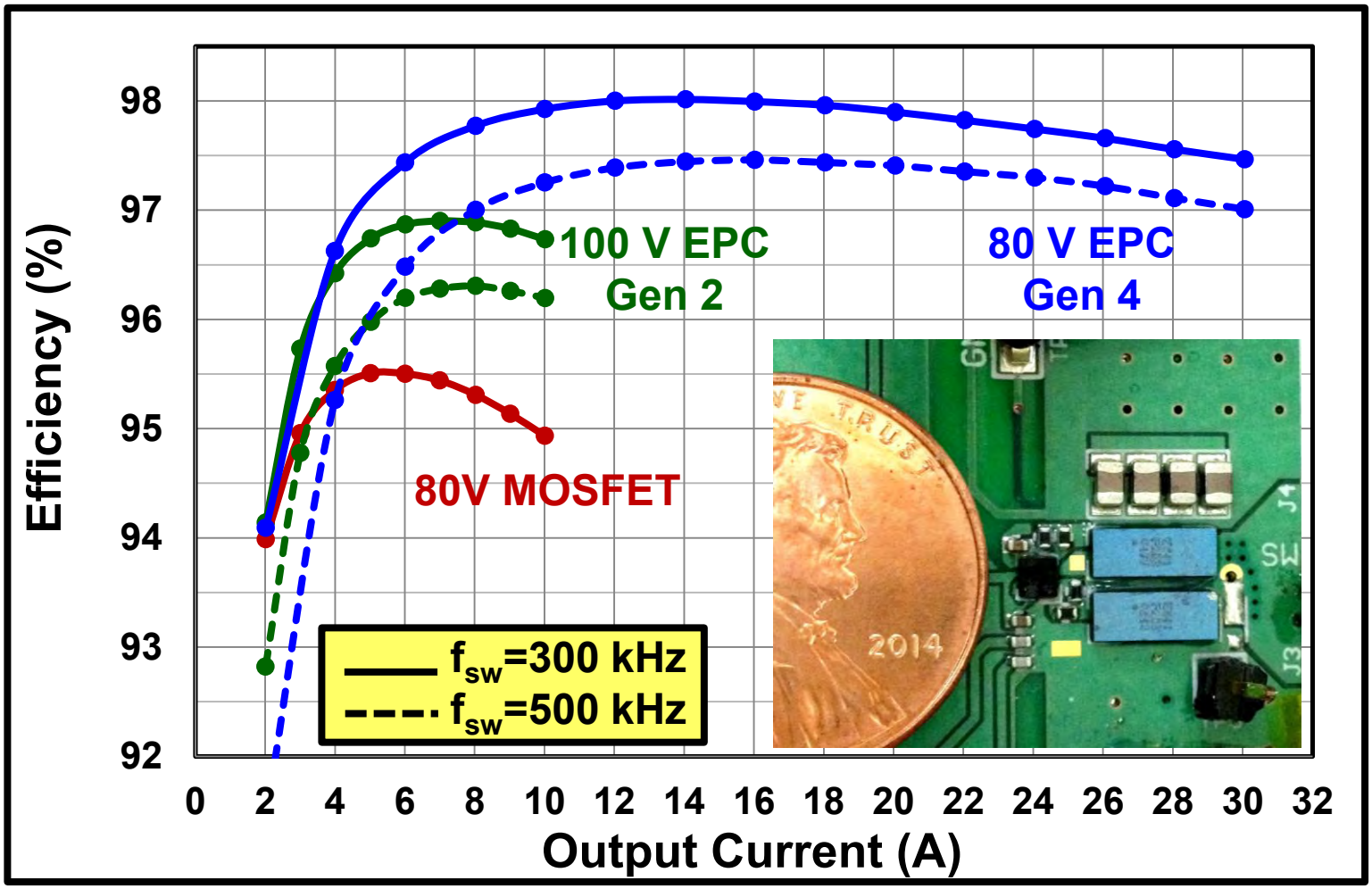





$V_{IN}$=48 V $V_{OUT}$=12 V Fully Regulated IBC

# Higher Current Devices

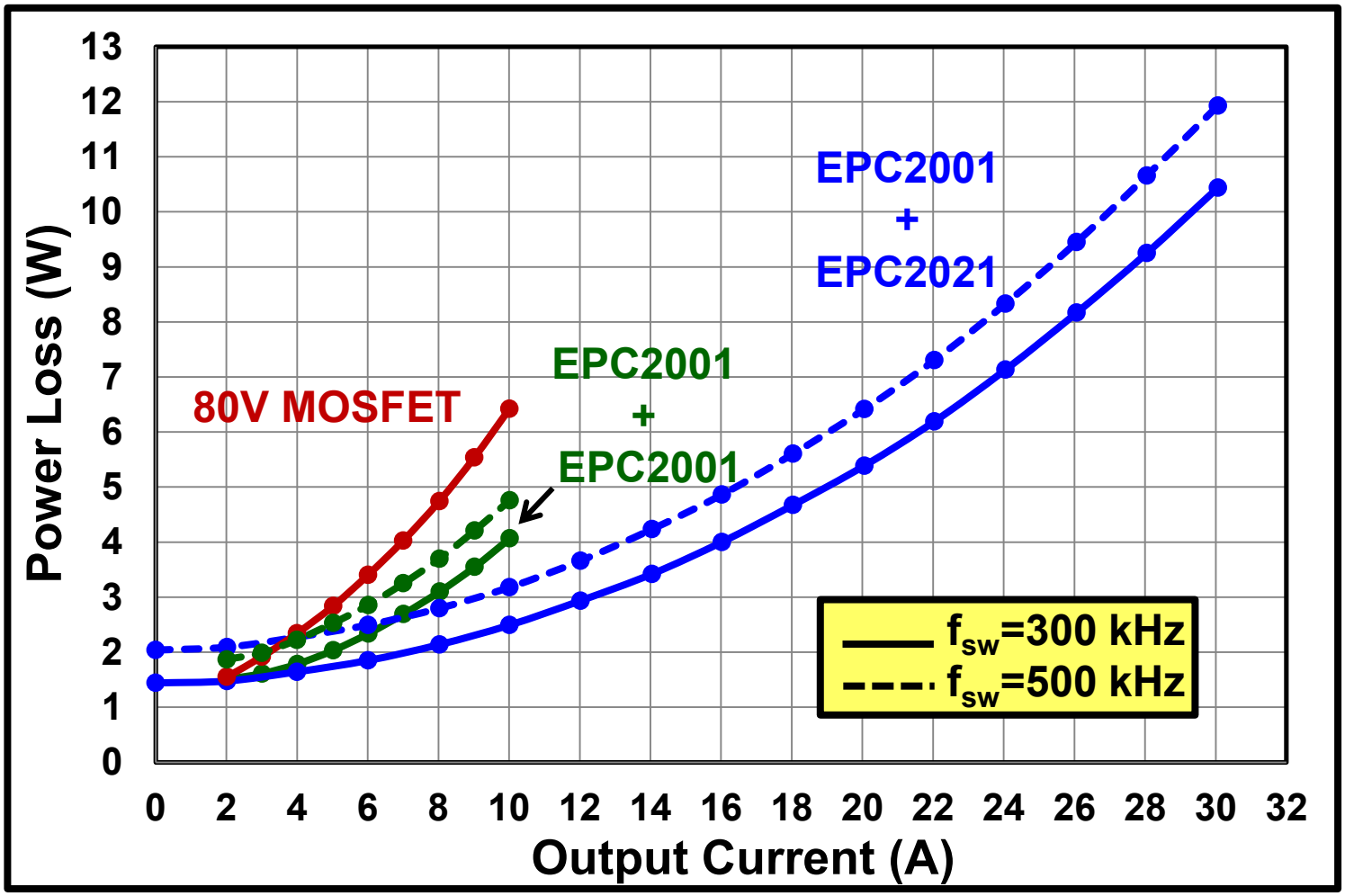





$V_{IN}$=48 V $V_{OUT}$=12 V

# Higher Current Devices

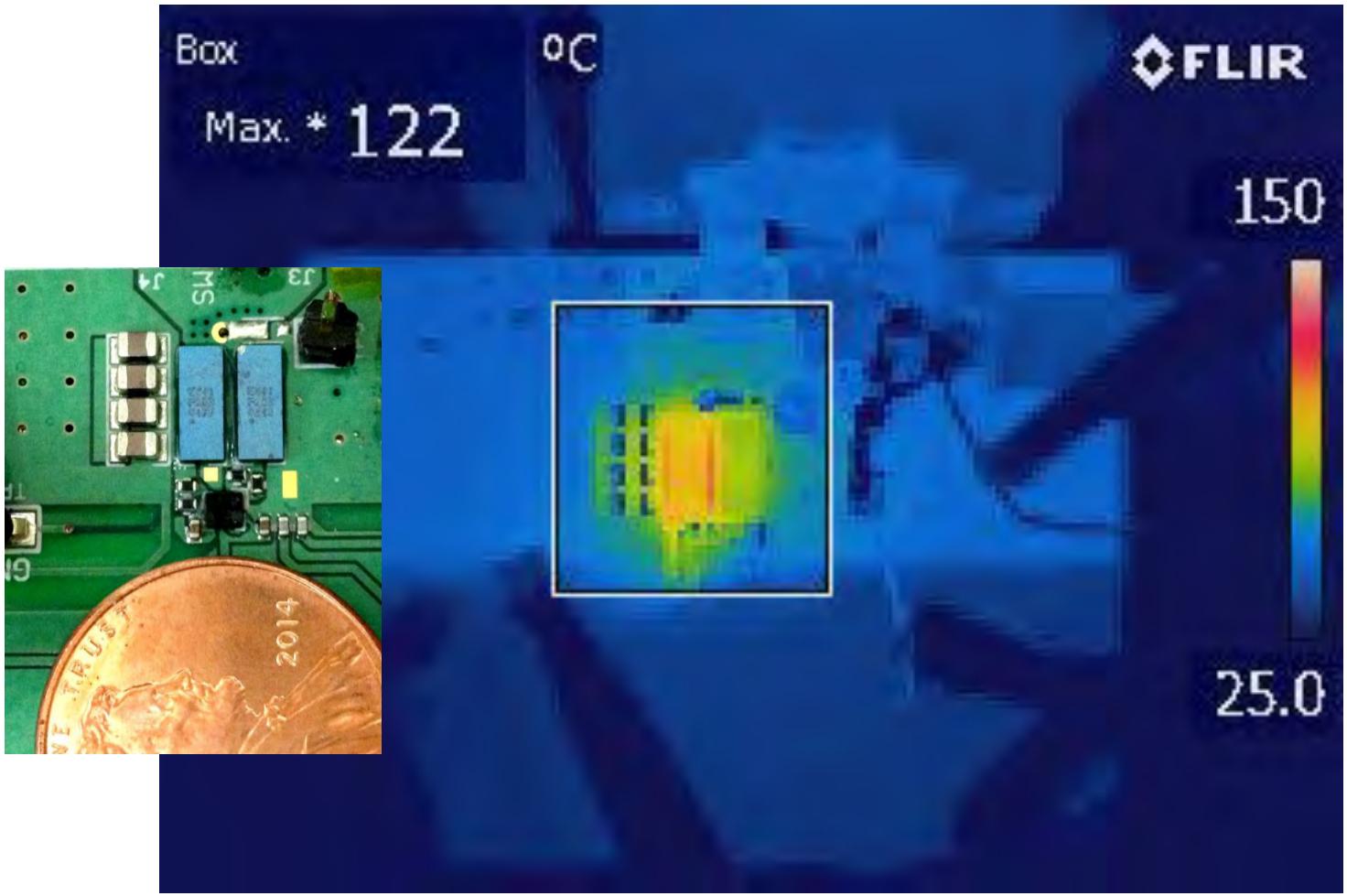





$V_{IN}$=48 V $V_{OUT}$=12 V

# Improved Thermal Performance



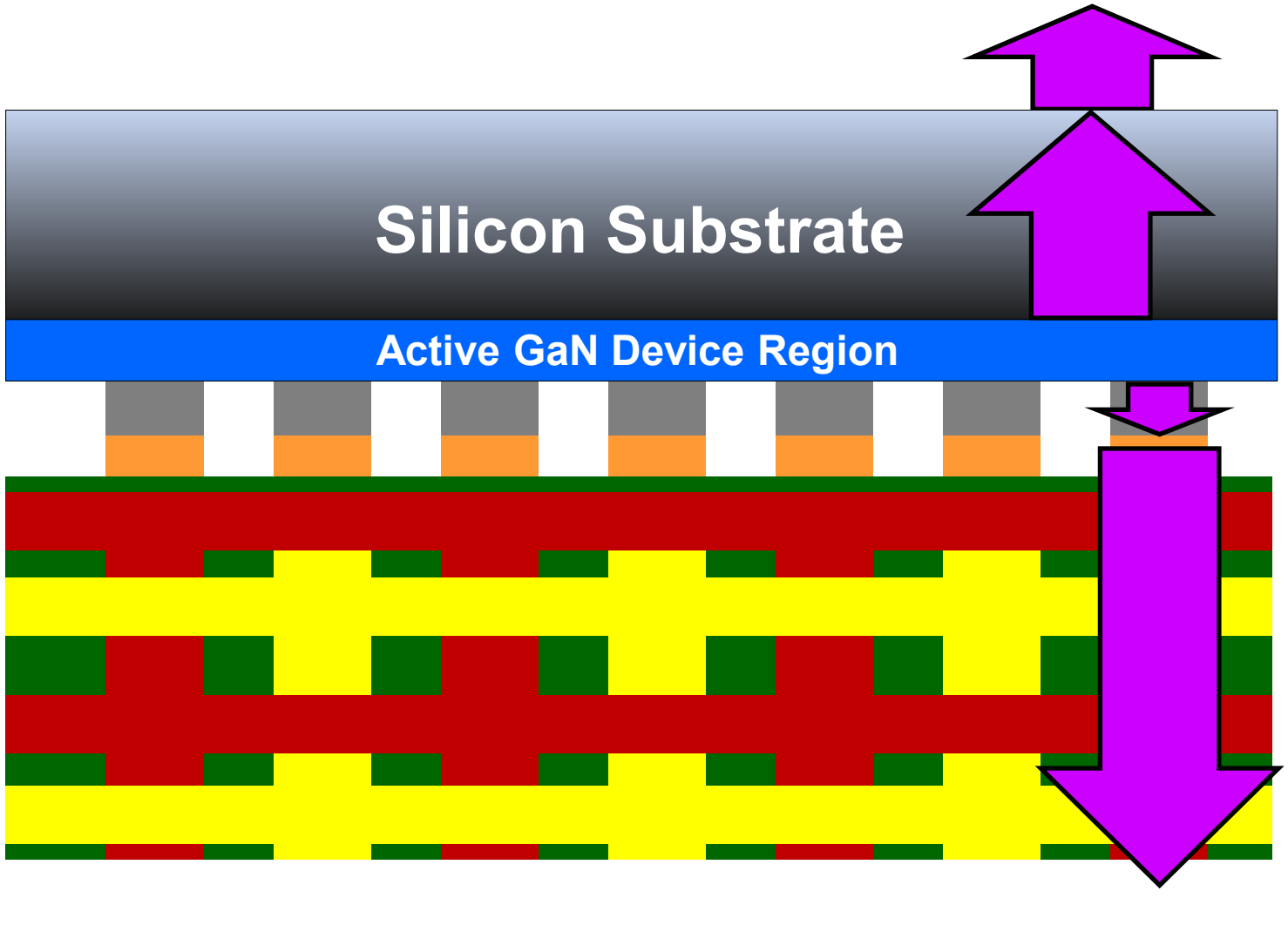


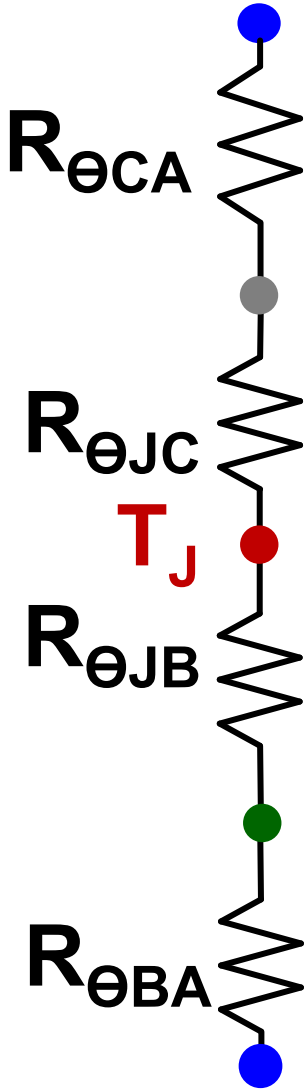

Fan Speed=200 LFM $f_{sw}$=300 kHz $V_{IN}$=48 V $V_{OUT}$=12 V $I_{OUT}$=30 A

# Thermal

# Thermal Management



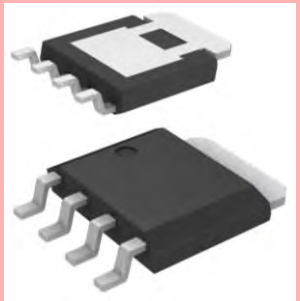


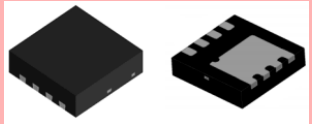



# Packaging Advancements



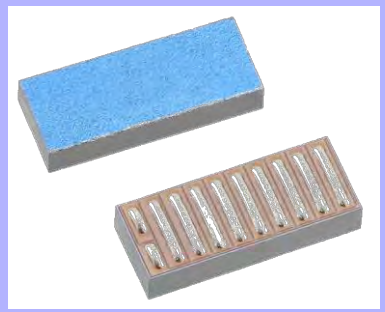
## Single Sided Cooling

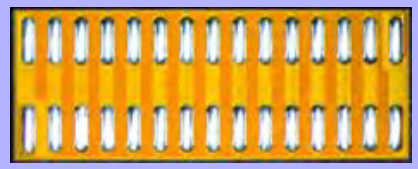




## Double Sided Cooling

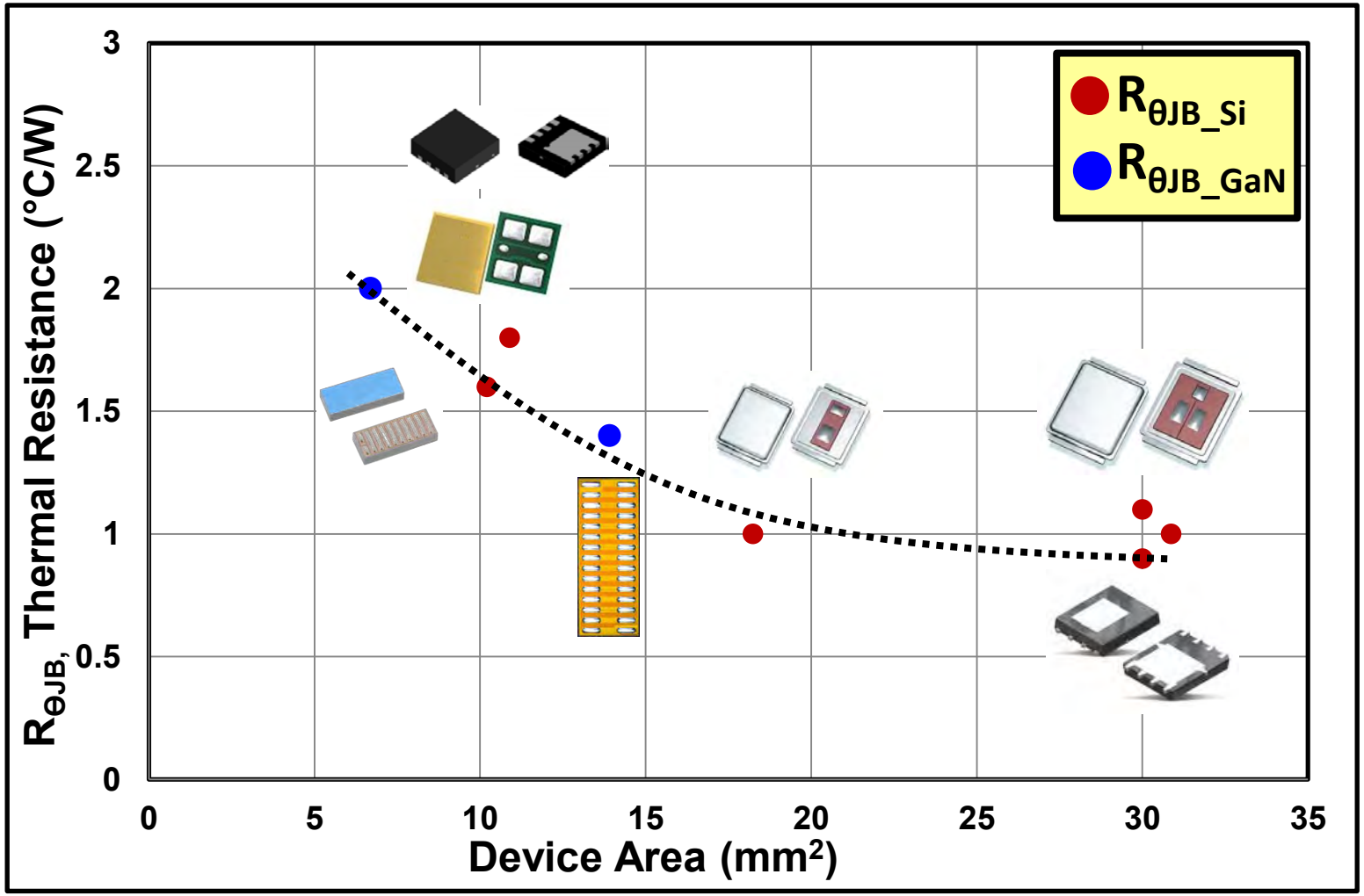
## Double Sided Cooling





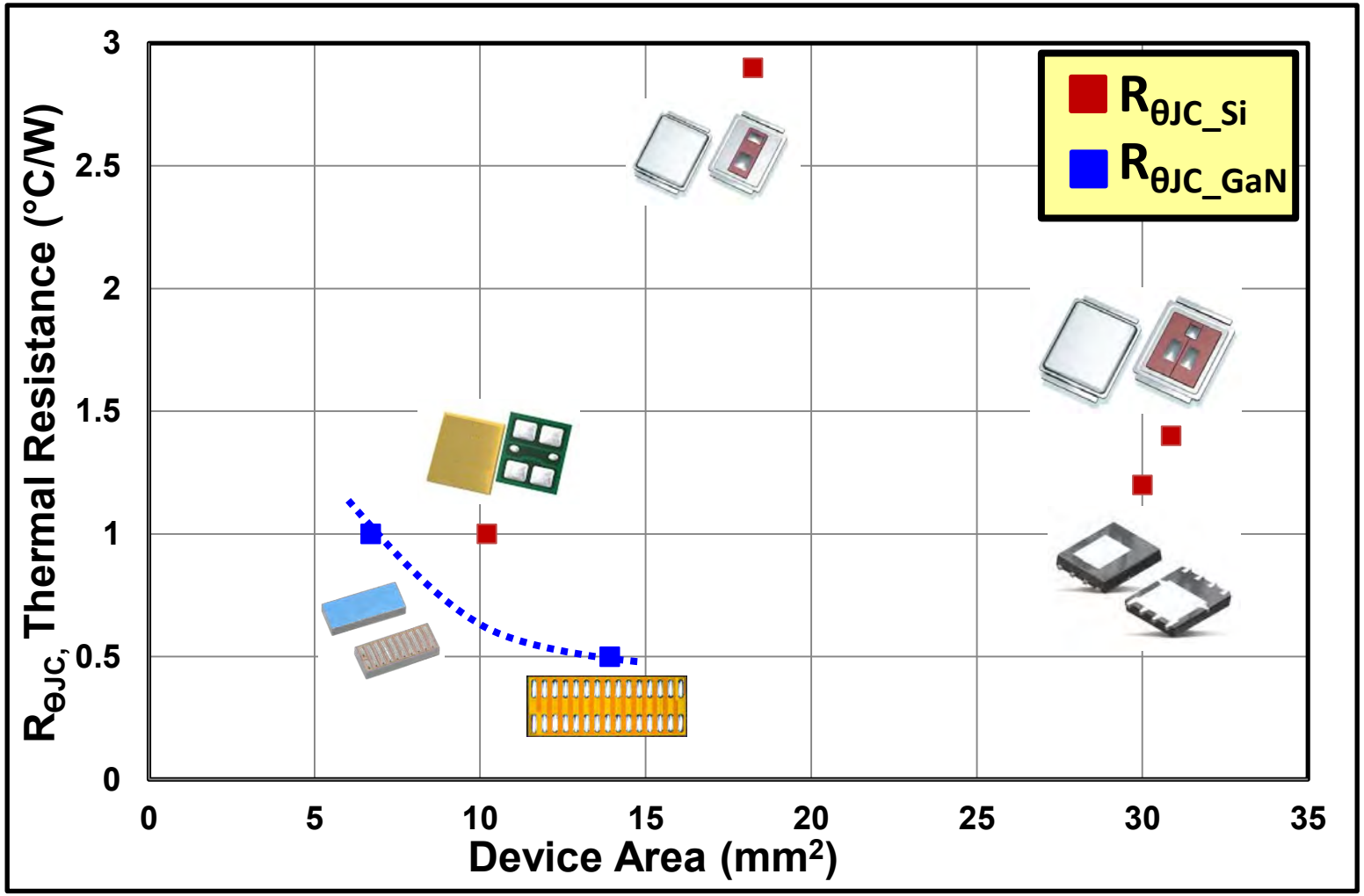
$R_{\Theta JB}\downarrow << R_{\Theta JC}\uparrow$ $R_{\Theta JB}\downarrow R_{\Theta JC}\downarrow$ $R_{\Theta JB}\downarrow R_{\Theta JC}\downarrow$

# Package Comparisons



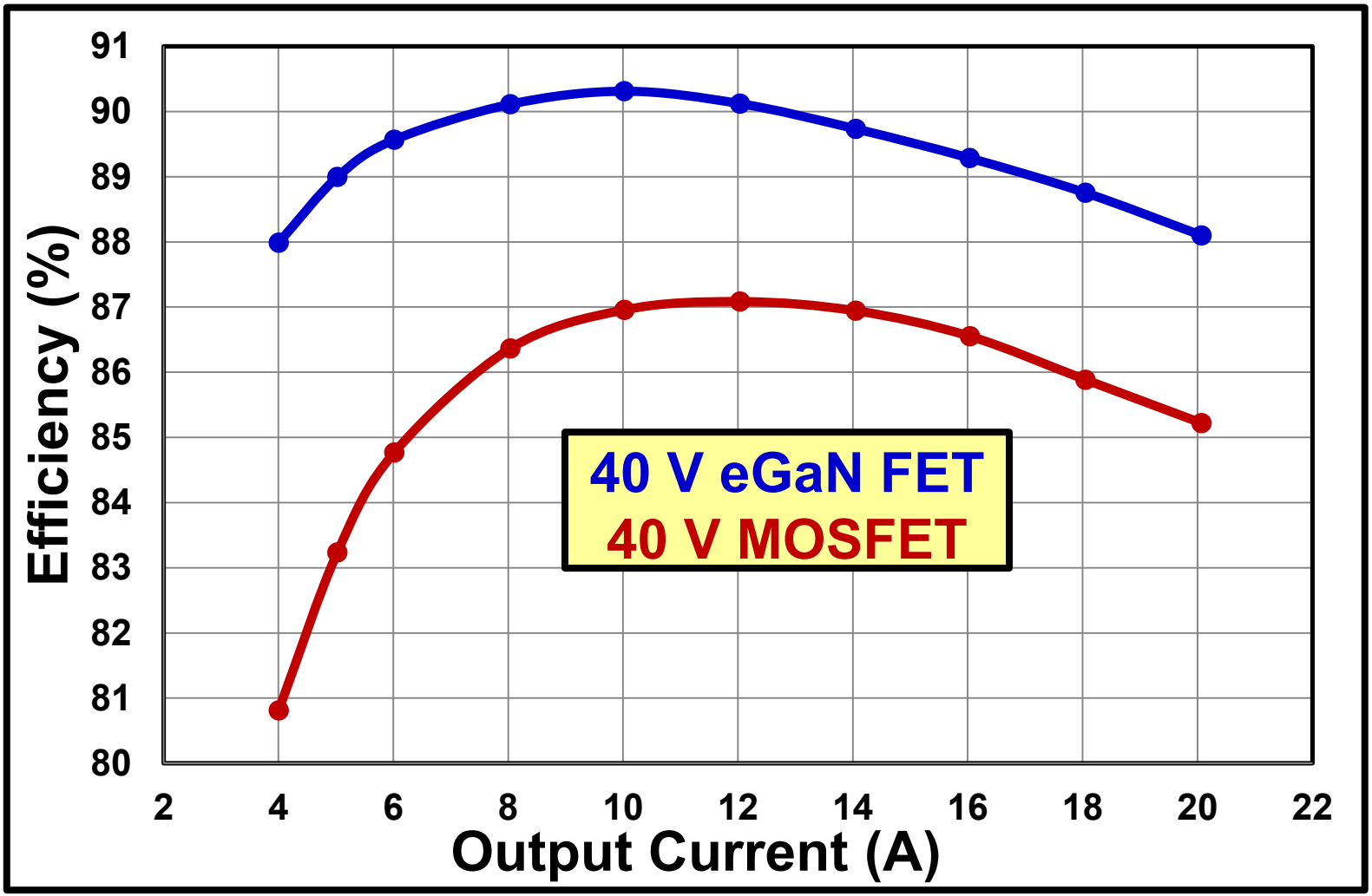
# Package Comparisons





# Performance Comparison

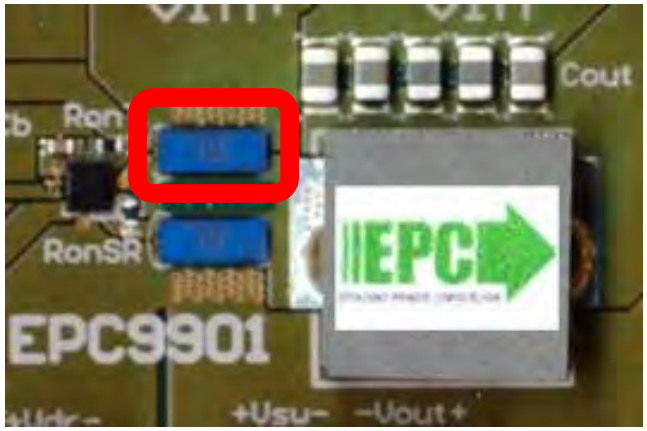




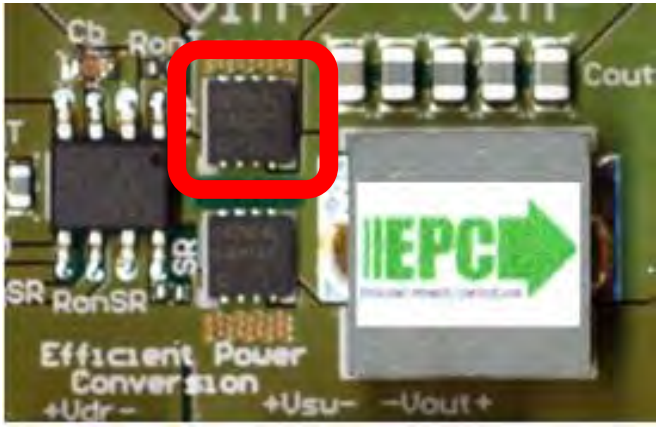

$V_{IN}$=12 V, $V_{OUT}$=1.2 V, $f_{sw}$=1 MHz, L=300 nH

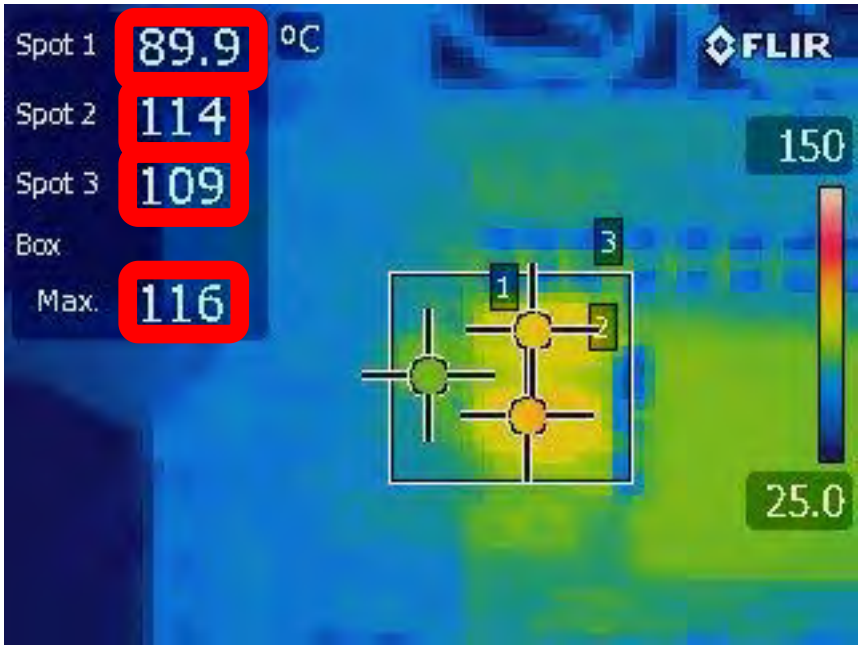
# Thermal Comparison

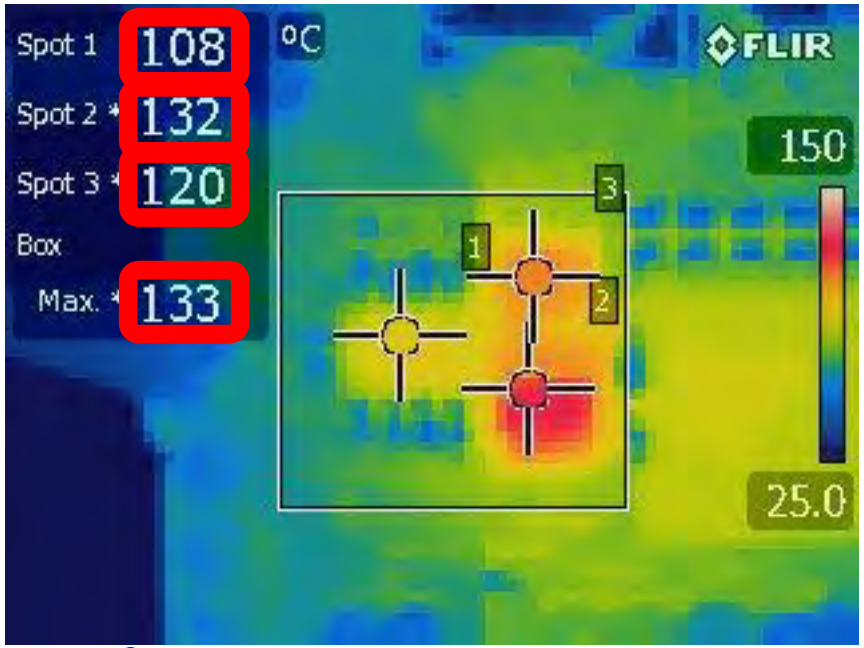





**GaN is**
**38% Smaller**
**13% Cooler**



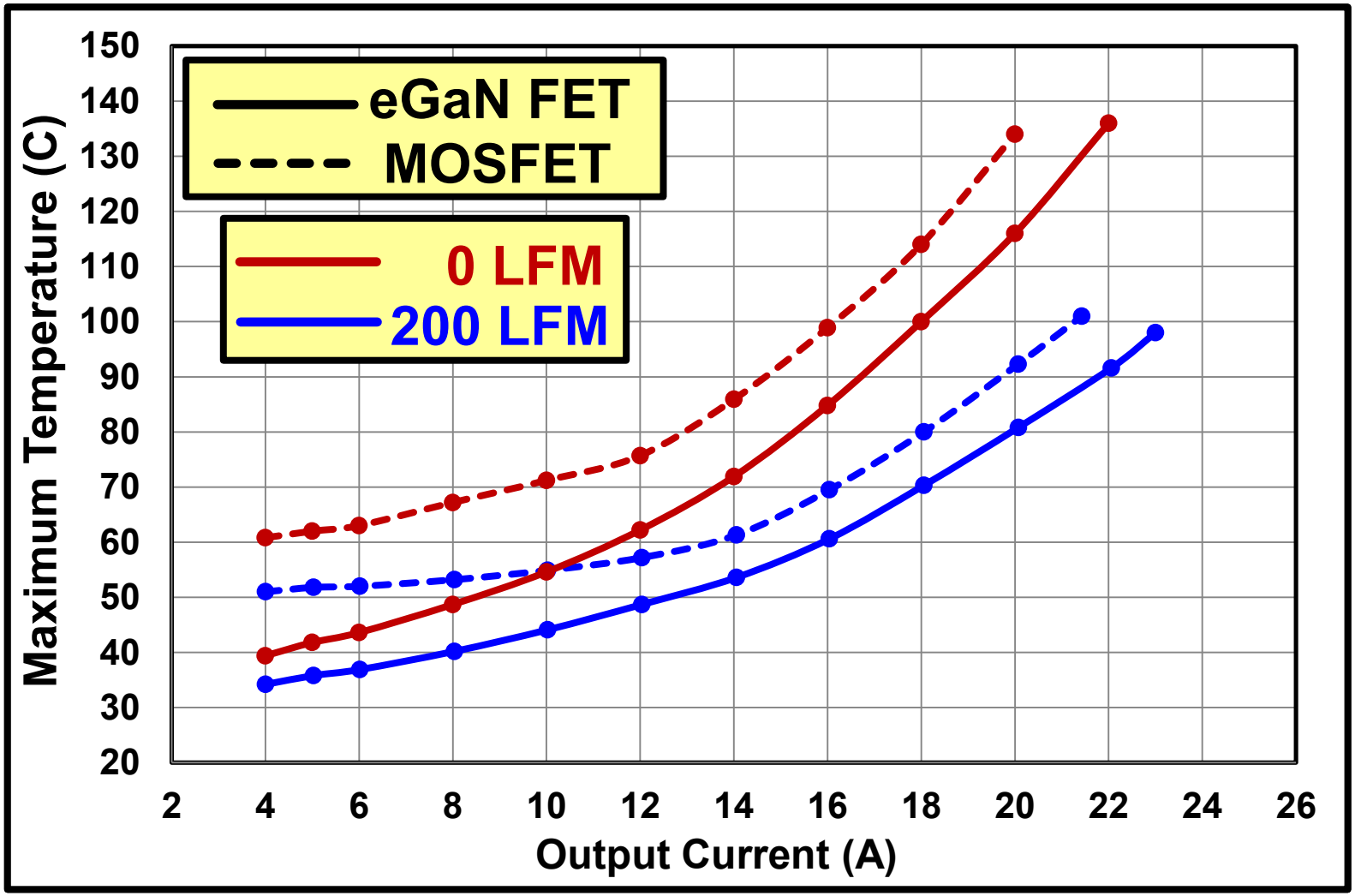




$V_{IN}$=12 V, $V_{OUT}$=1.2 V, $I_{OUT}$=20 A, $f_{sw}$=1 MHz, L=300 nH

# Thermal Comparison

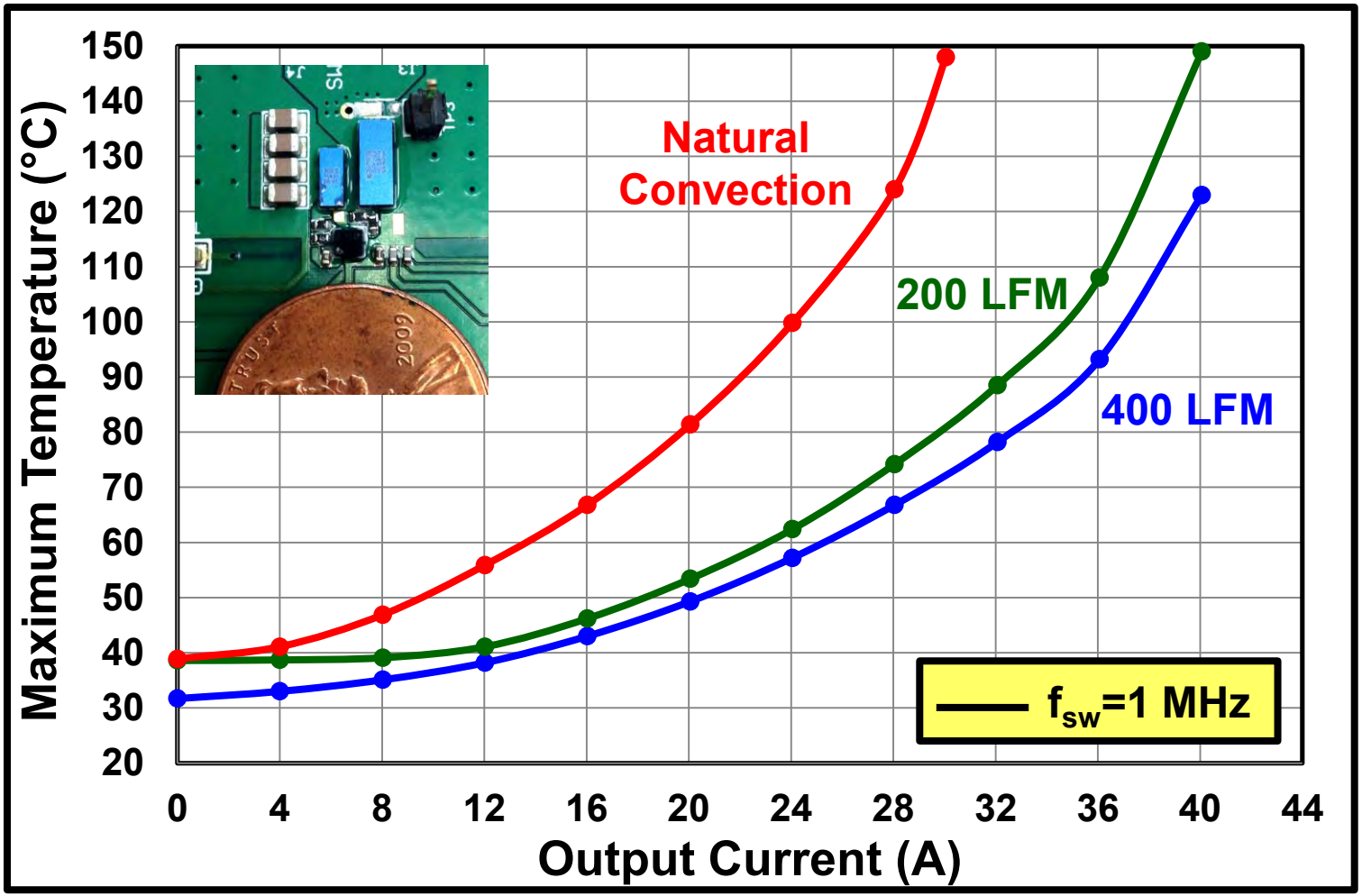





$V_{IN}$=12 V, $V_{OUT}$=1.2 V, $f_{sw}$=1 MHz, L=300 nH

# Generation 4 Thermal Performance

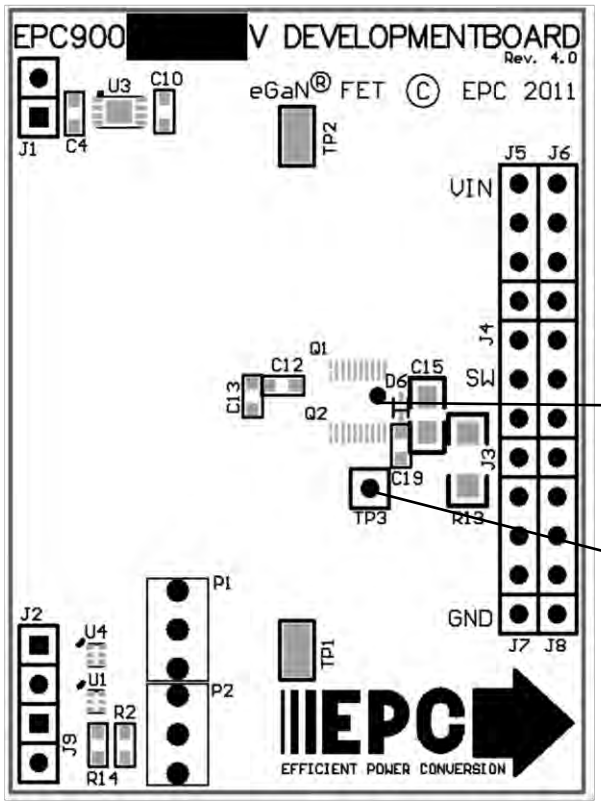


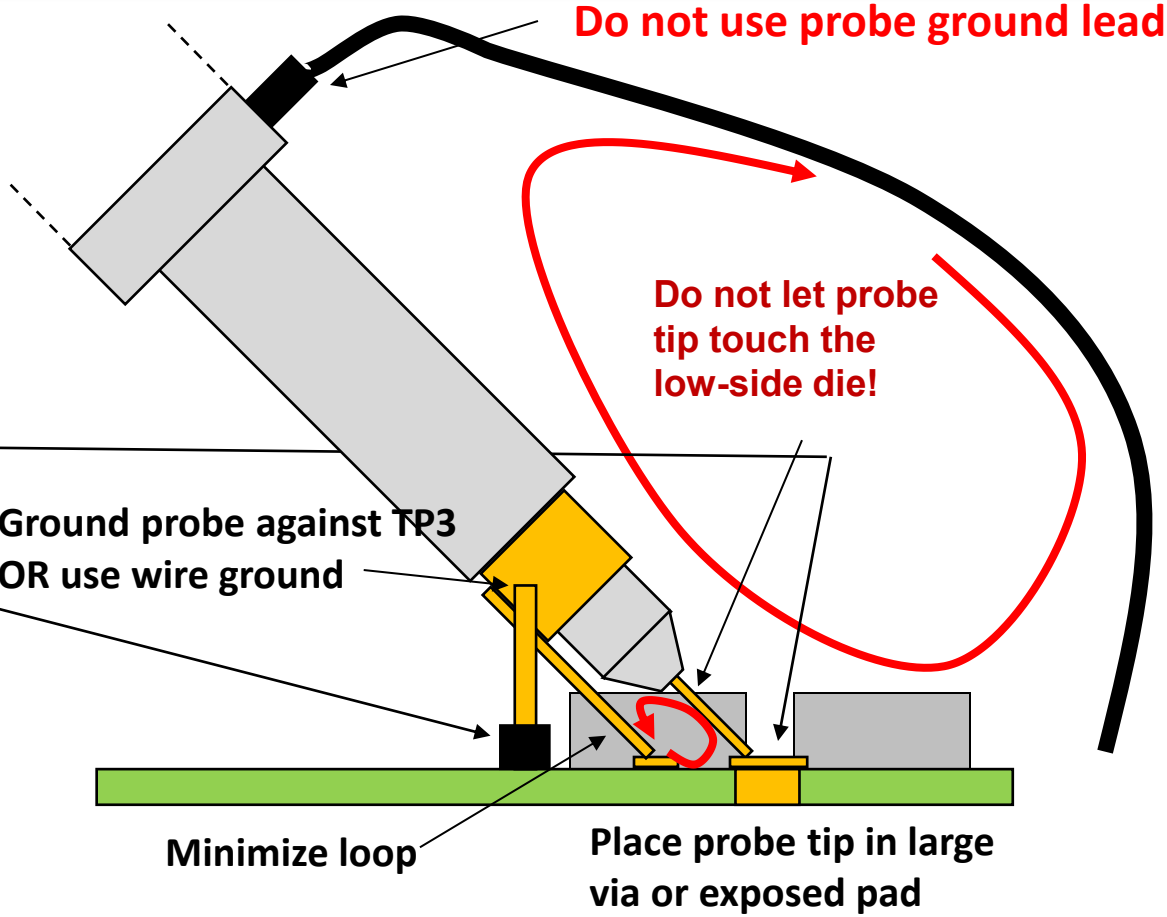



$V_{IN}$=12 V $V_{OUT}$=1.2 V

# Measurement

# Voltage Measurement

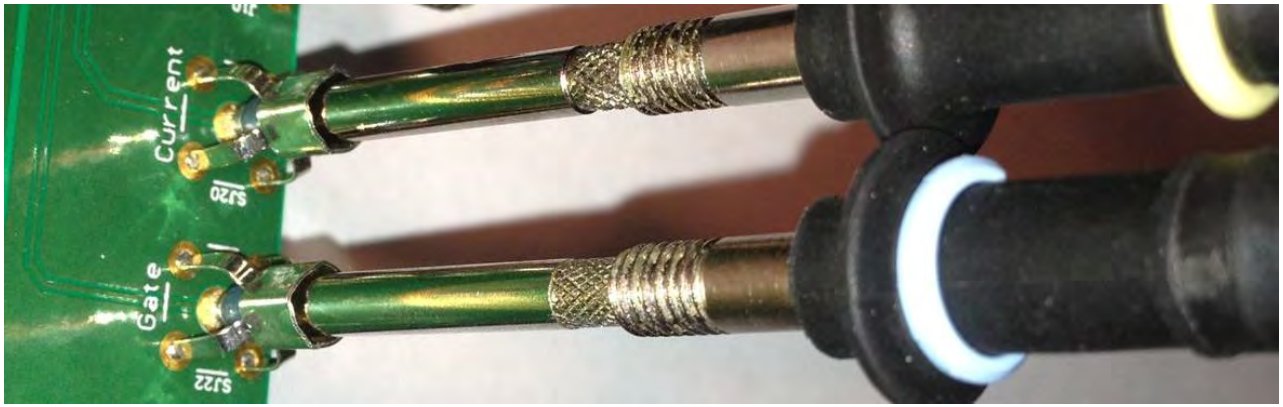


# Probe Options



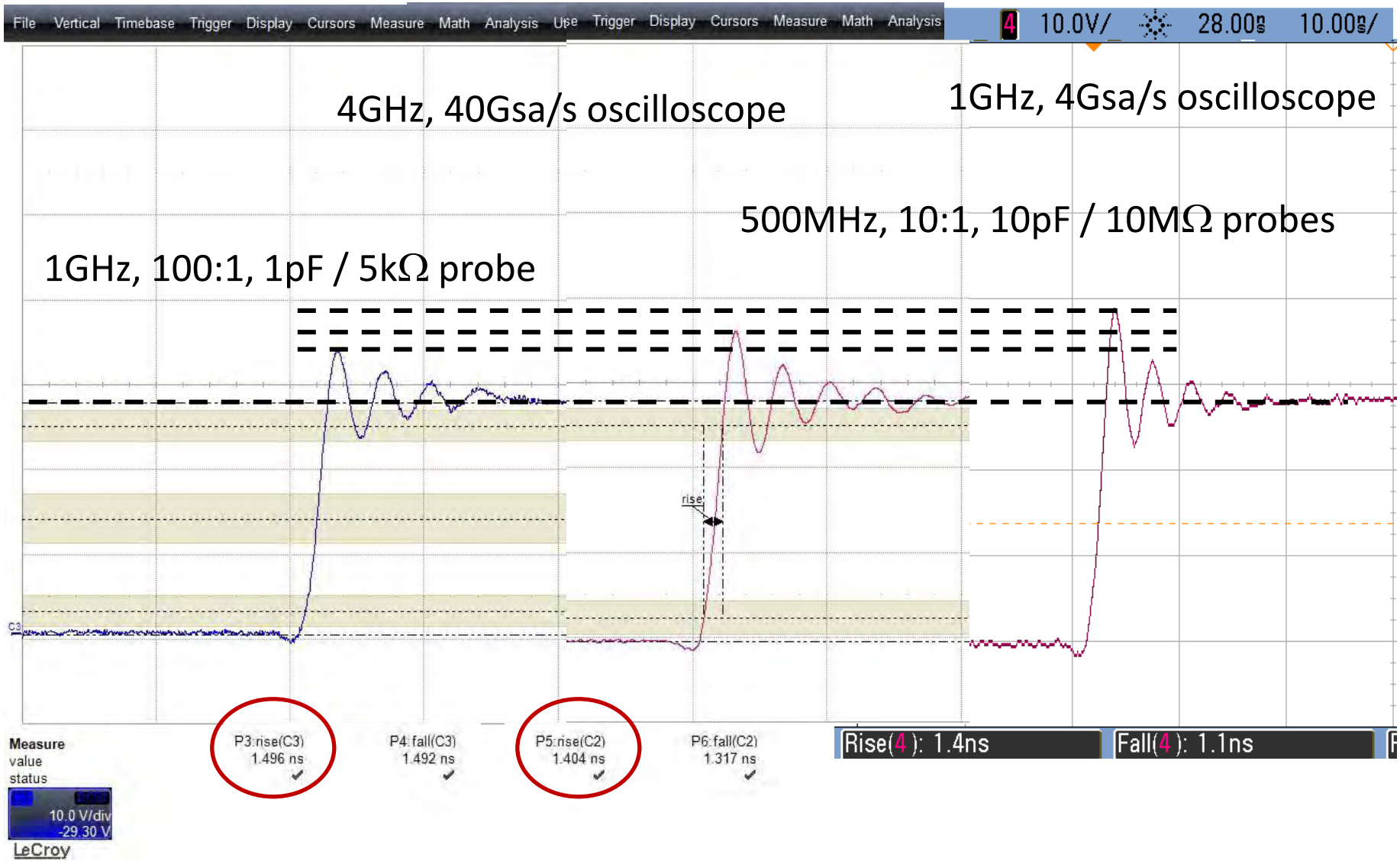
## Tektronix PCB Jack




Yokogawa Probe

Hand-made Probe Adapter

# High Speed Measurement



# Design Basics Summary



- *eGaN FETs raise the bar for power conversion performance*
- **Lower resistance per die area**
- **Better FOM's**
- **Better Packaging**
- **Improved PCB Layout Techniques**
  - **Superior In-Circuit Performance**
  - **Can parallel devices for higher current**
- **Avoid gate overshoot and long dead-times**

# Design Examples

# Design Example Agenda



- Resonant Bus Converter
- Envelope Tracking
- Wireless Power
- LiDAR
- Class-D Audio

# Resonant Bus Converter

# Figure of Merit (FOM) History

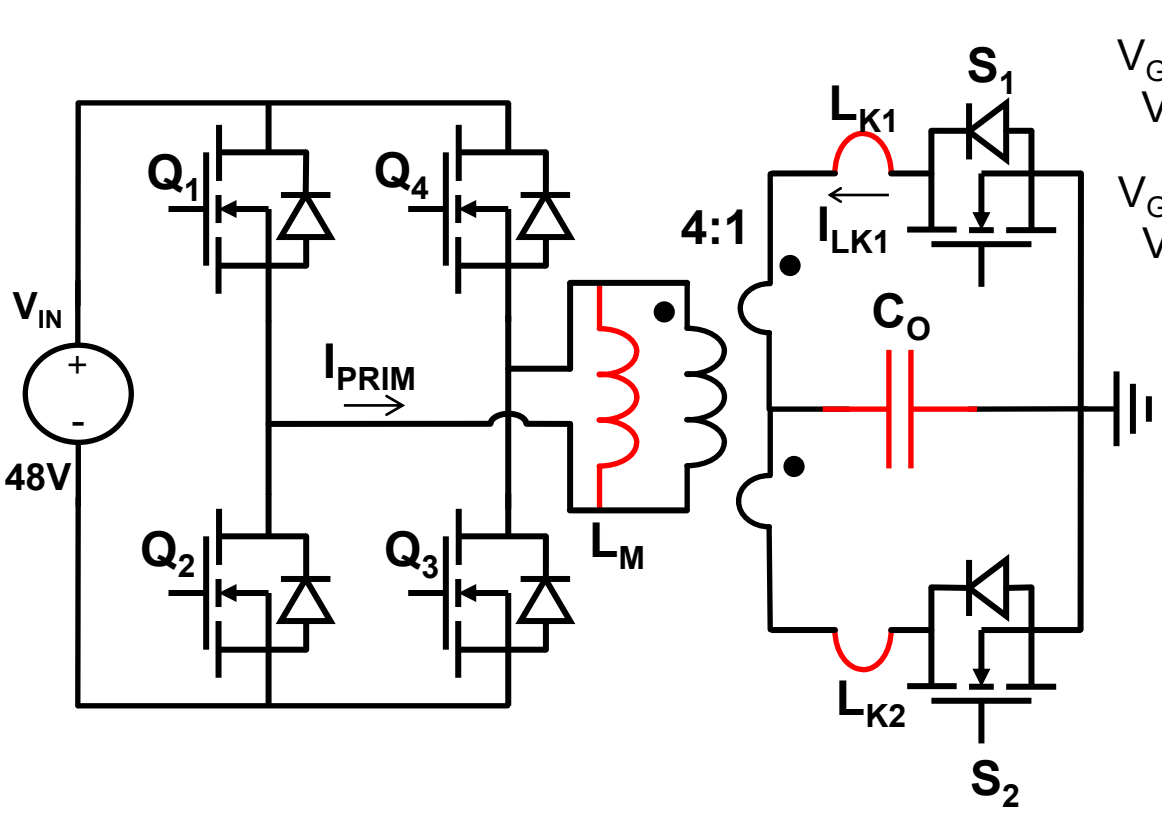


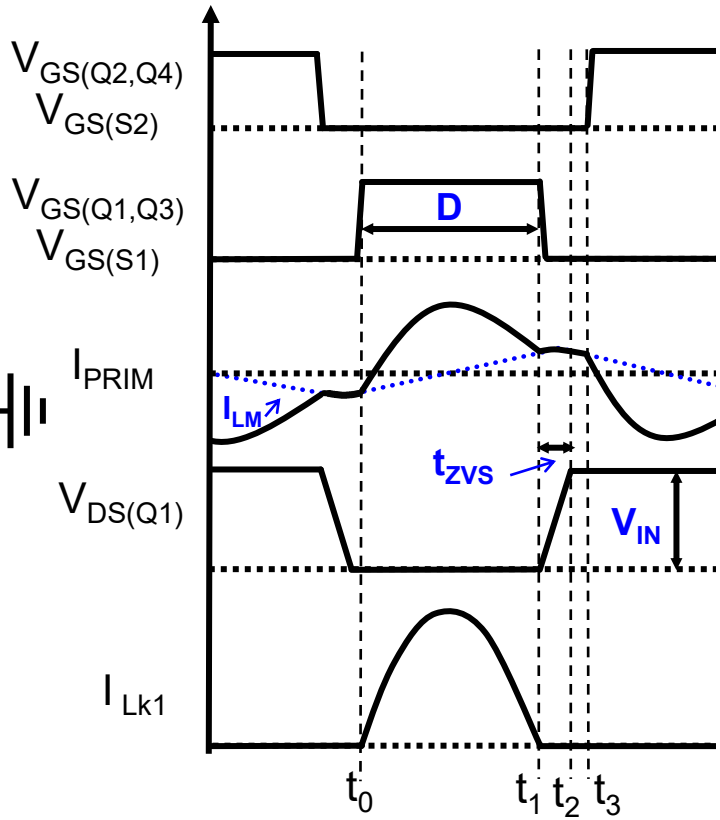
- In 1989, Baliga derived a switching FOM
  - $\mathbf{BHFFOM} = \frac{1}{R_{ON,SP} \cdot C_{IN,SP}}$
- In 1995, Kim et al proposed a new FOM
  - $\mathbf{NHFFOM} = \frac{1}{R_{ON,SP} \cdot C_{OSS,SP}}$
- In 2004, Huang proposed a new FOM
  - $\mathbf{HDFOM} = \sqrt{R_{ON,SP} \cdot Q_{GD,SP}}$

# Resonant Bus Converter



## High Frequency DC/DC Transformer

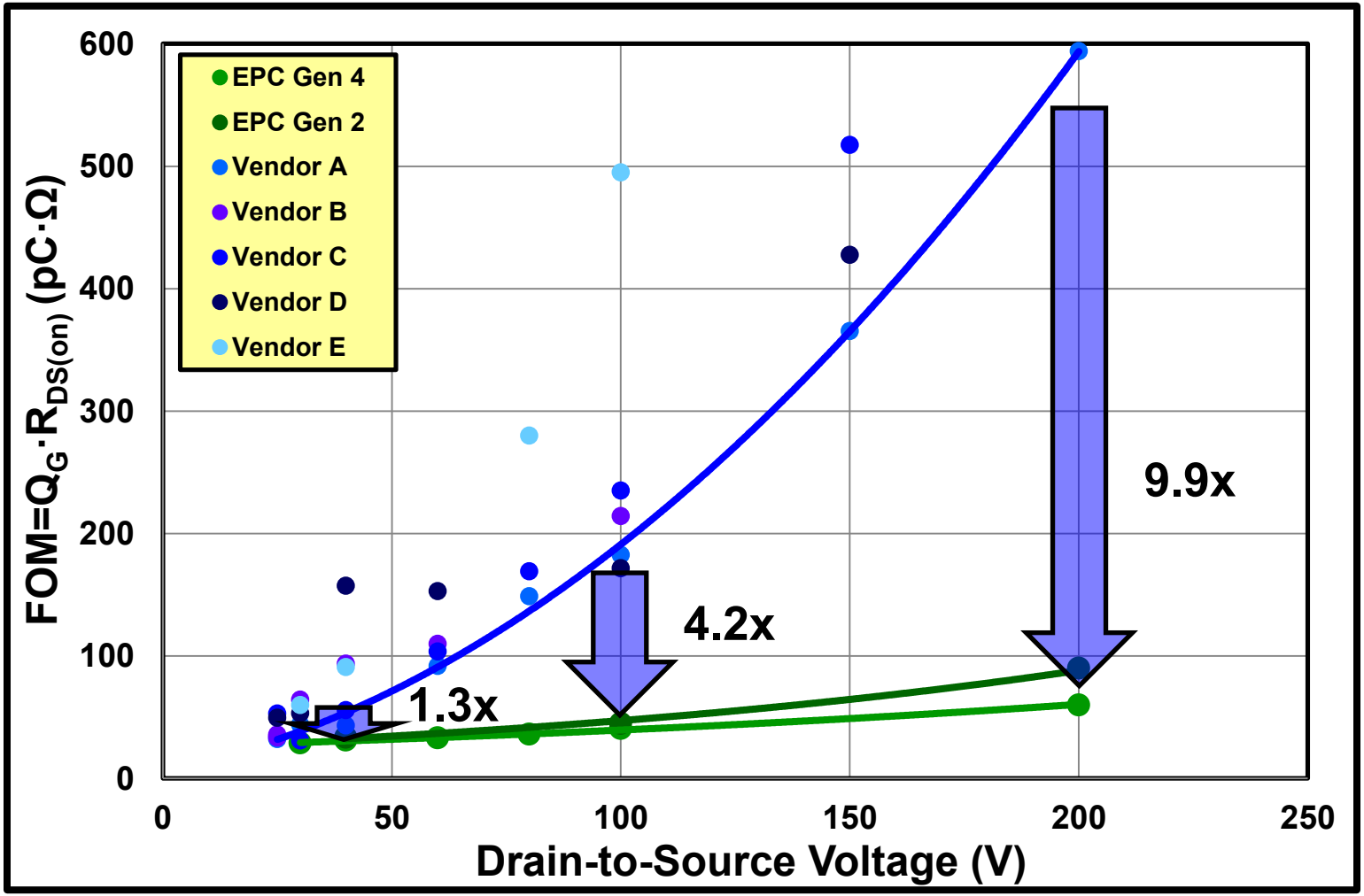



Ref: Y. Ren, M. Xu, J. Sun, and F. C. Lee, "A family of high power density unregulated bus converters," IEEE Trans. Power Electron., vol. 20, no. 5, pp. 1045–1054, Sep. 2005.

# Gate Charge Figure of Merit

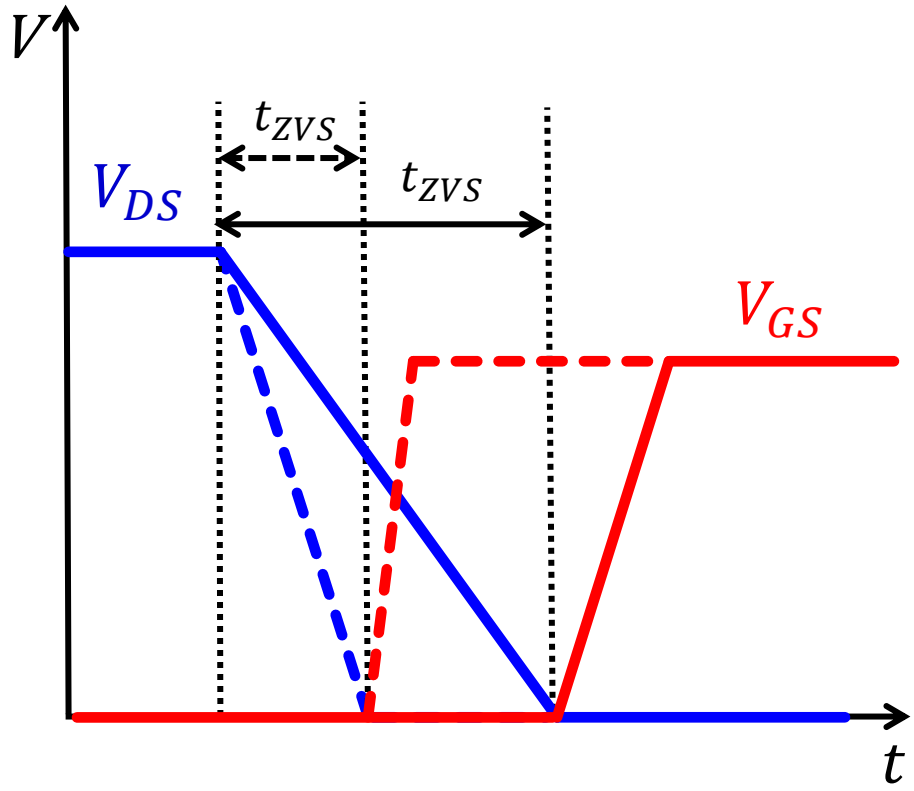


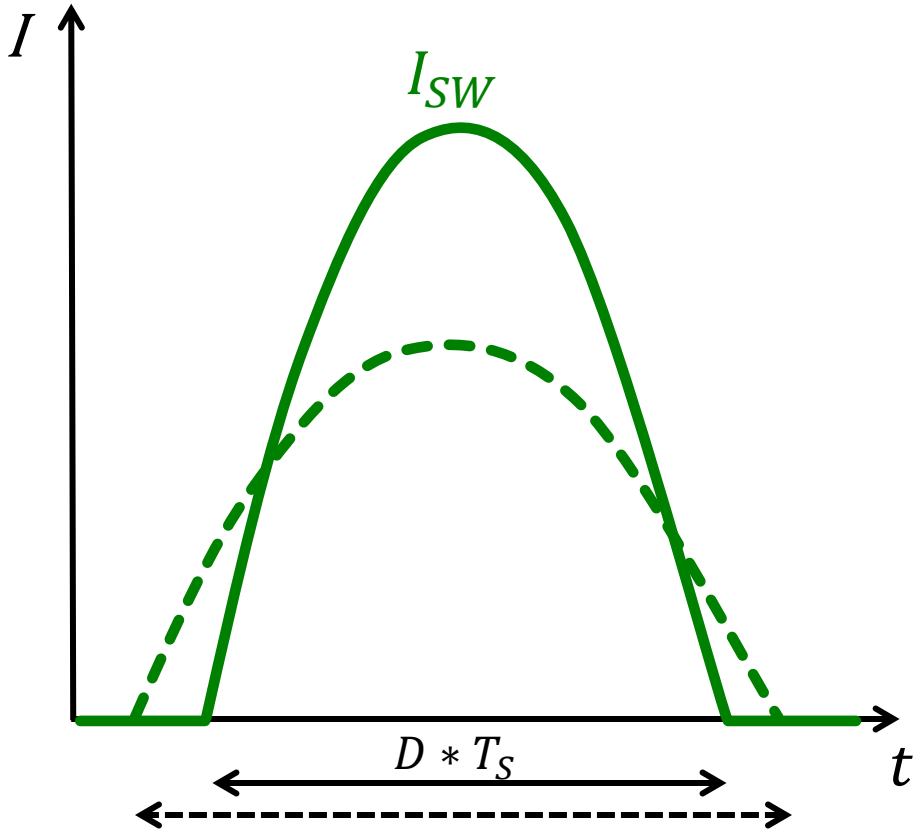


# Output Charge



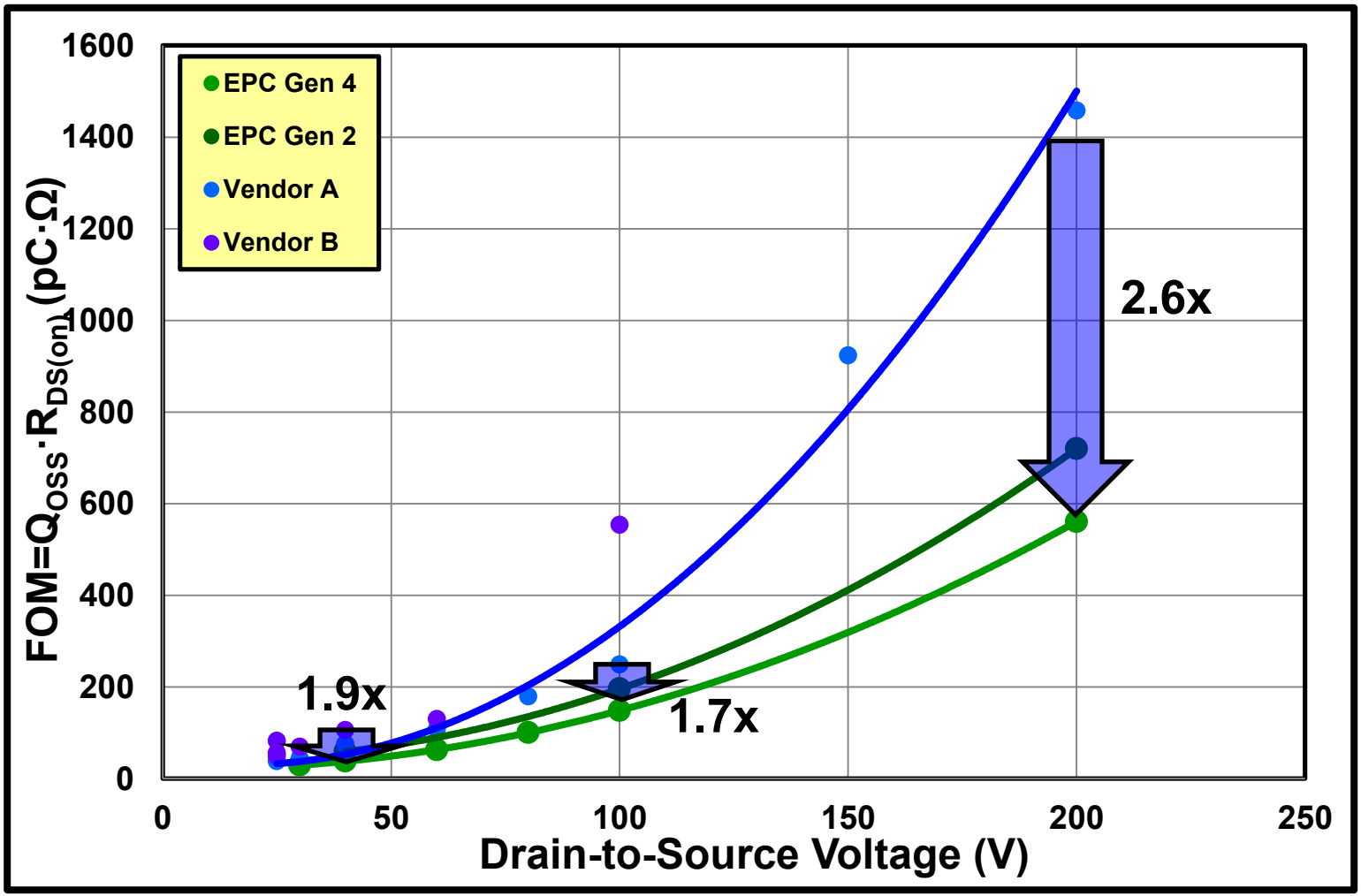
$Q_{OSS}$ ↓ $t_{ZVS}$ ↓ $I_{RMS}$ ↓ $P_{CON}$ ↓



# Output Charge FOM

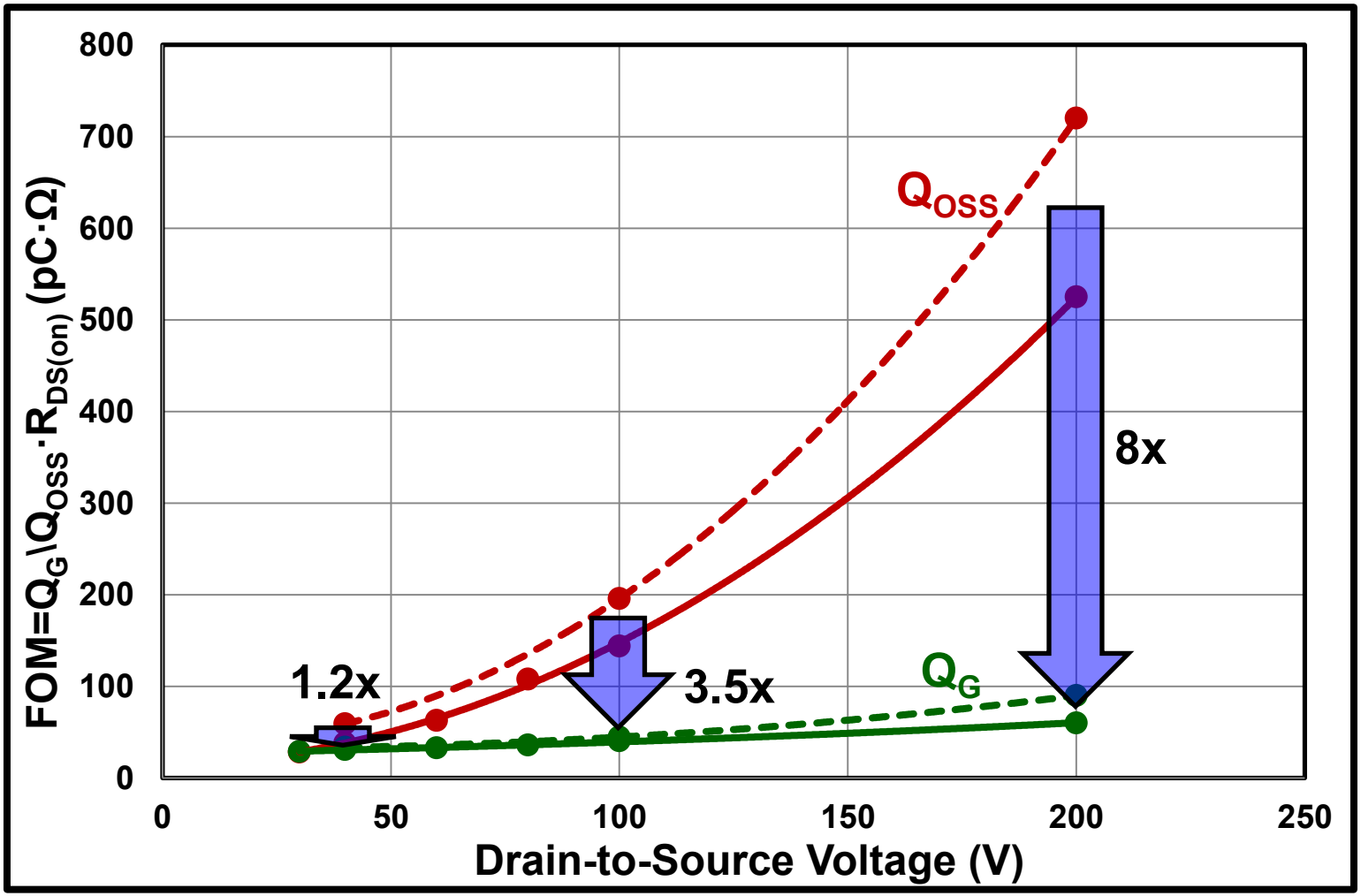





$V_{DS}=0.5 \cdot V_{DSS}$

# Soft-Switching FOM

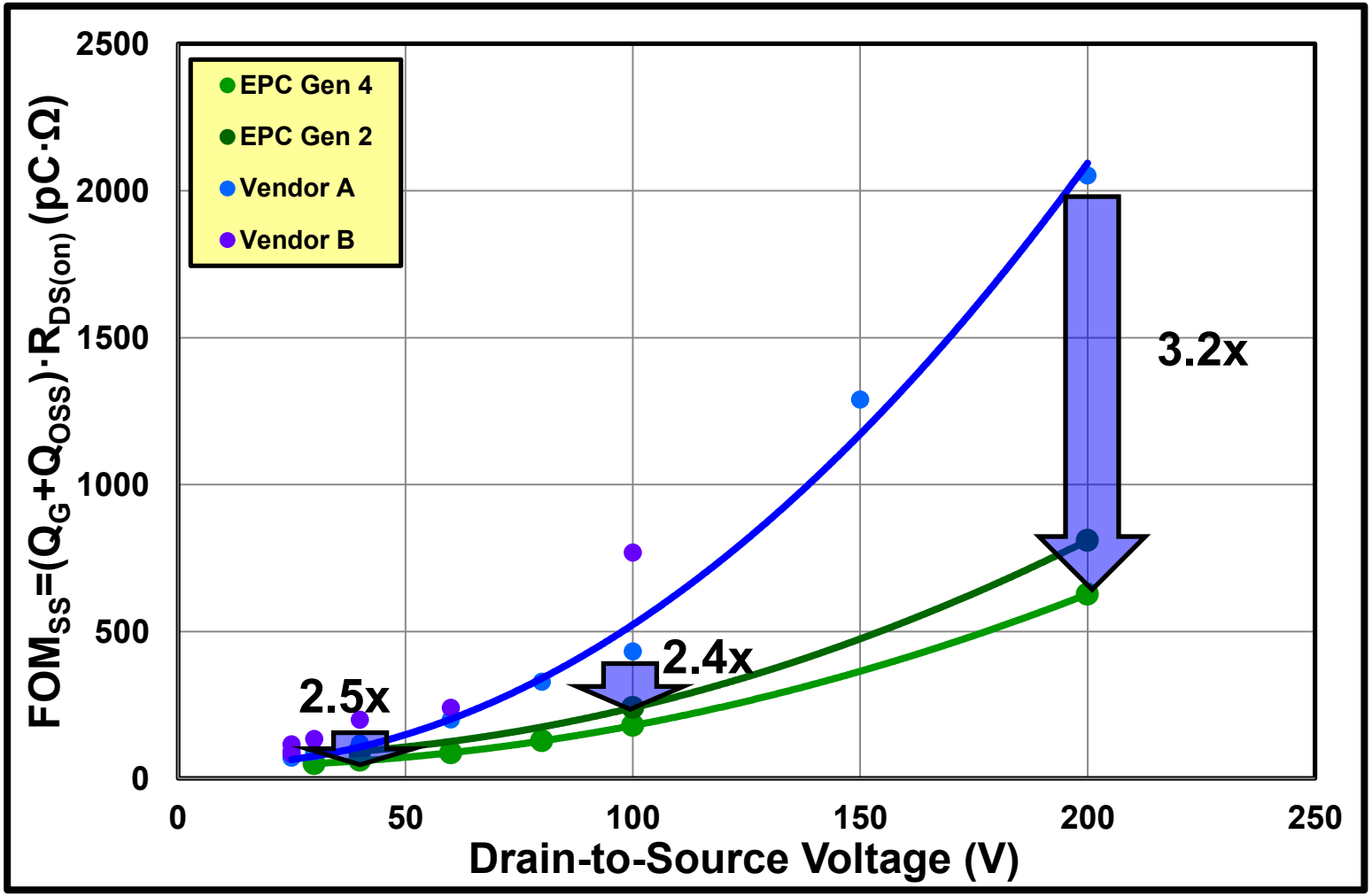





$$FOM_{SS} = (Q_{OSS} + Q_G) \cdot R_{DS(on)}$$

# Soft-Switching FOM

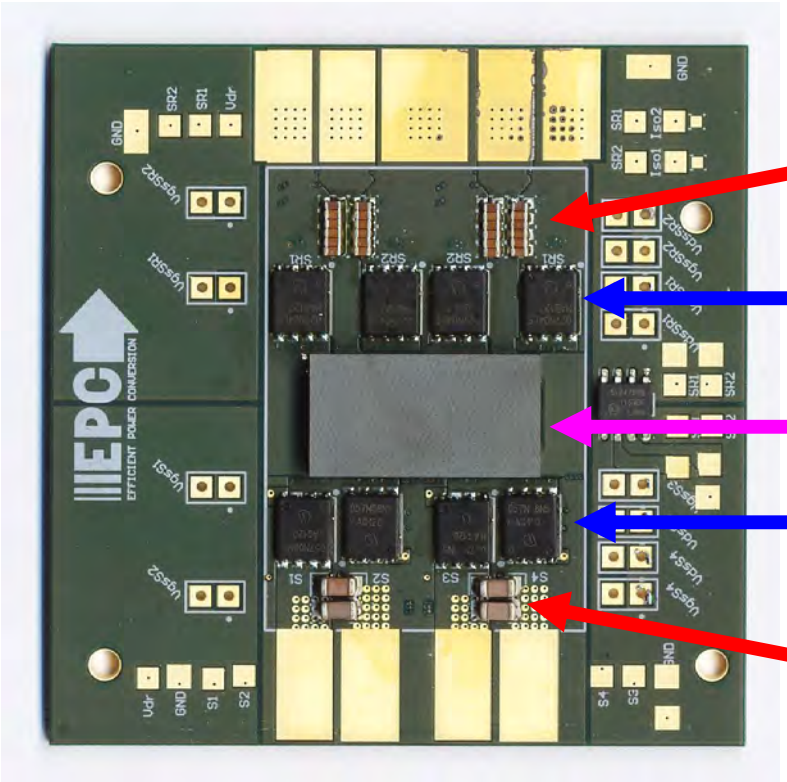





$$FOM_{SS} = (Q_{OSS} + Q_G) \cdot R_{DS(on)}$$

# eGaN FET vs. MOSFET





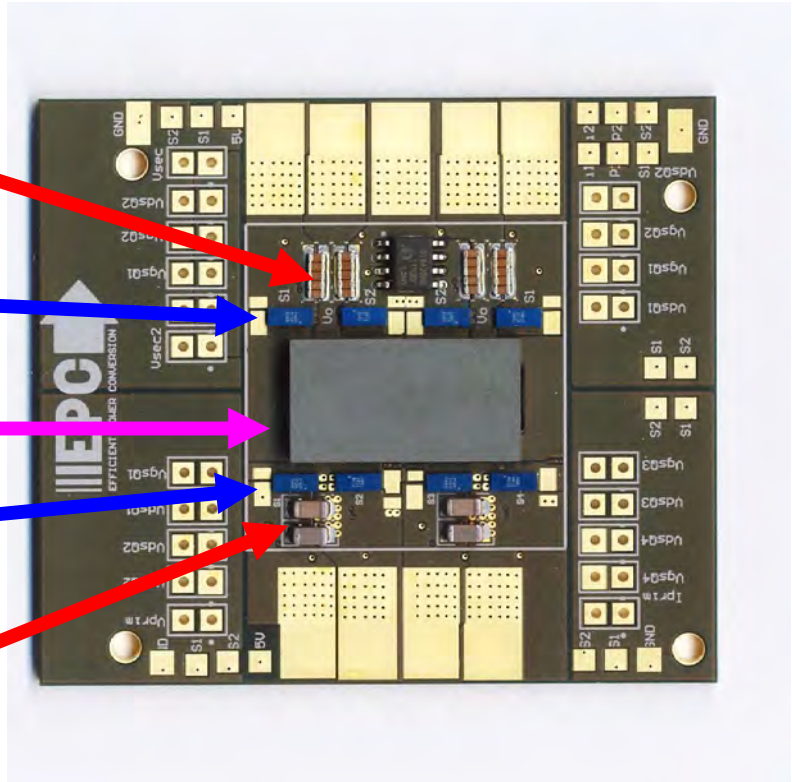
Resonant Capacitors

Secondary Devices

Transformer

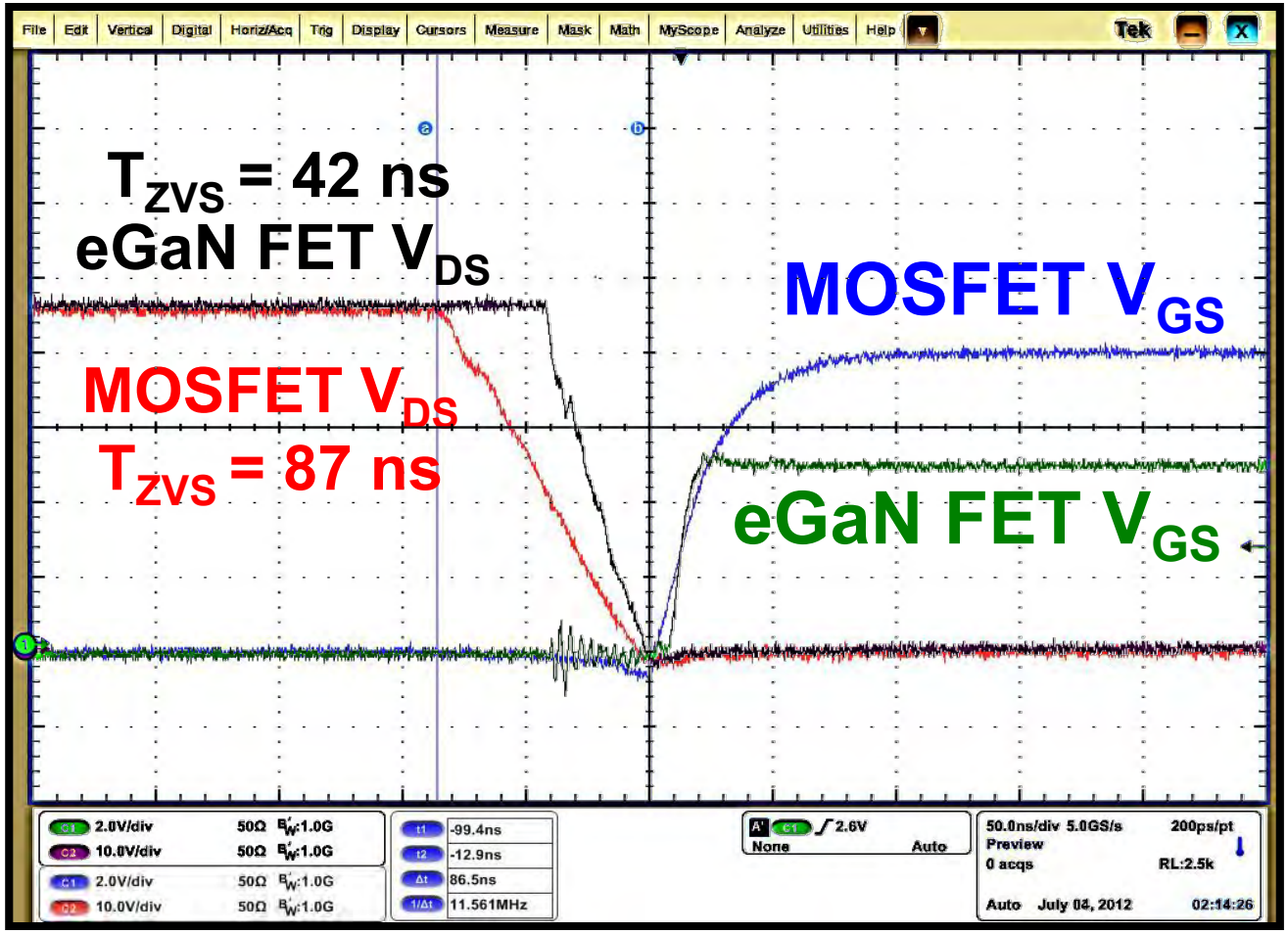
Primary Devices

Input Capacitors



**MOSFET** **vs.** **eGaN®FET**

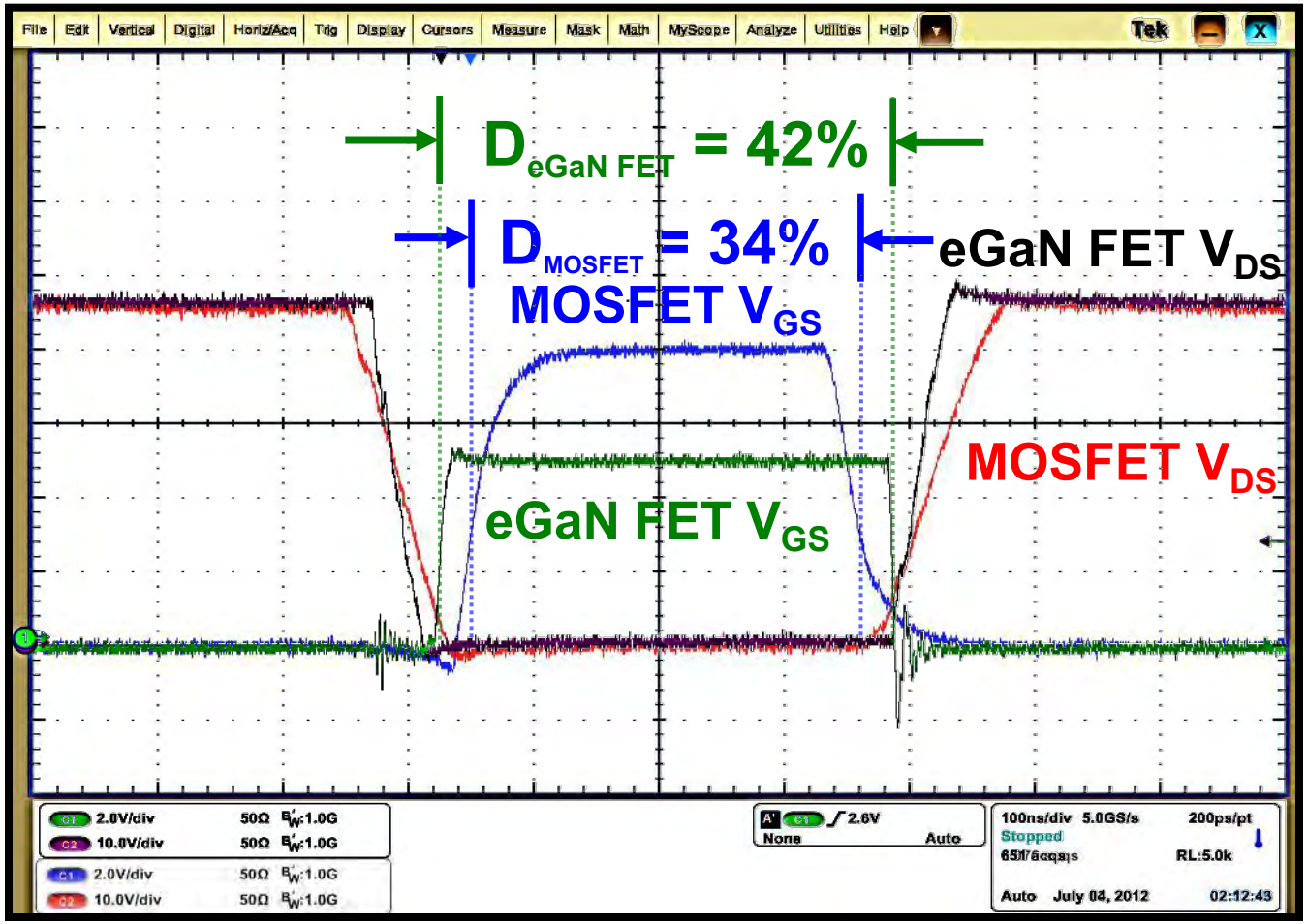
# ZVS Switching Comparison




$f_{sw}$ = 1.2 MHz, $V_{IN}$ = 48 V, and $V_{OUT}$ ≈ 12 V

# Duty Cycle Comparison

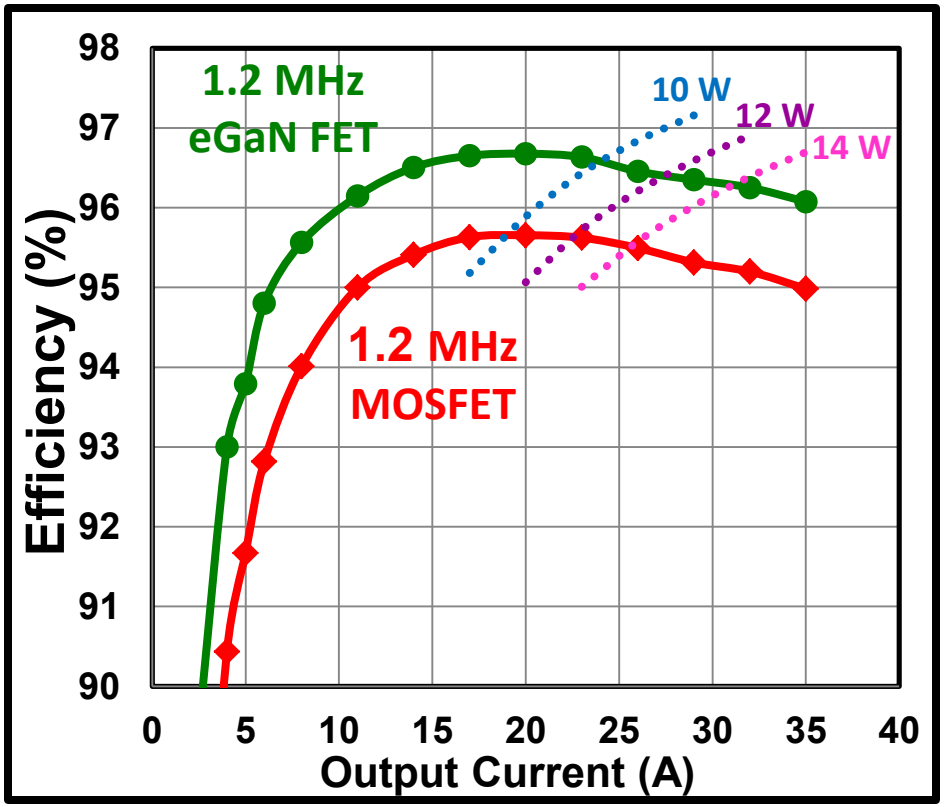


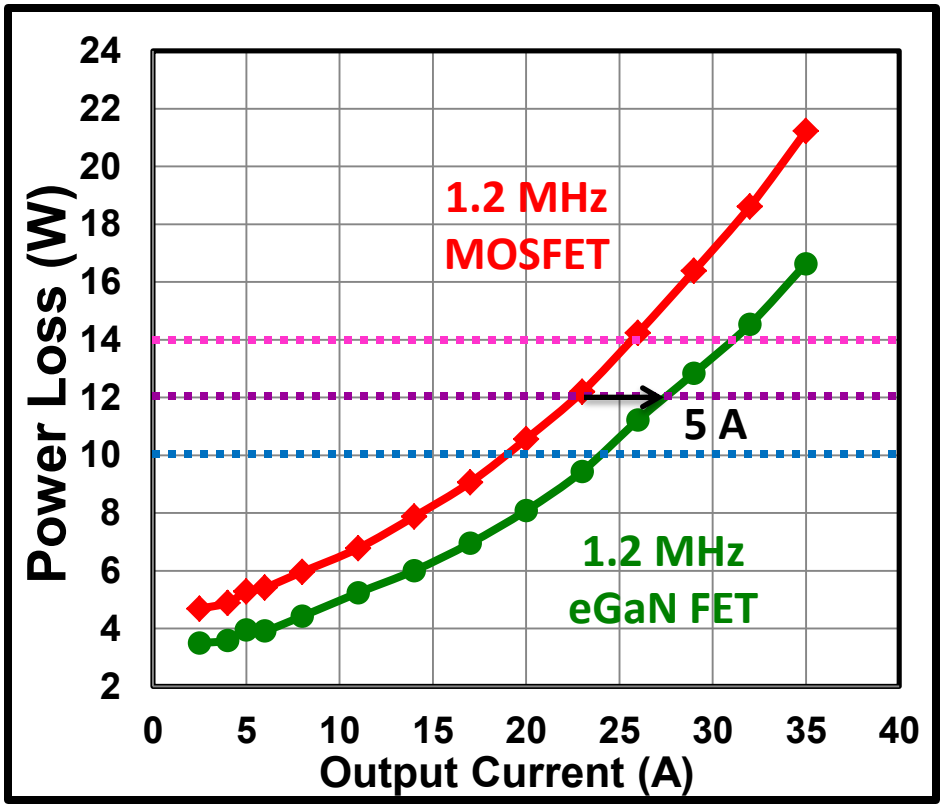



$f_{sw}$ = 1.2 MHz, $V_{IN}$ = 48 V, and $V_{OUT}$ ≈ 12 V

# Efficiency Comparison





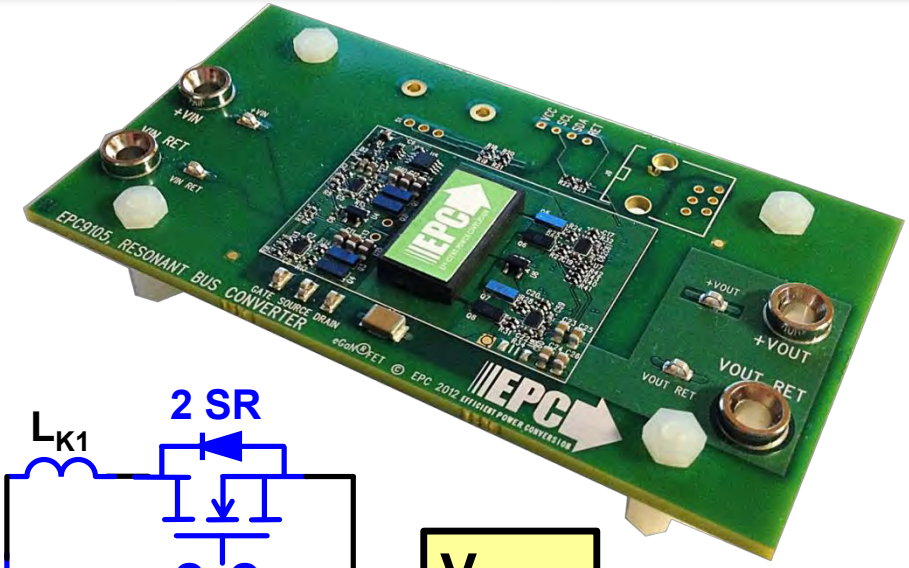

$f_{sw}$ = 1.2 MHz, $V_{IN}$ = 48 V, and $V_{OUT} \approx$ 12 V

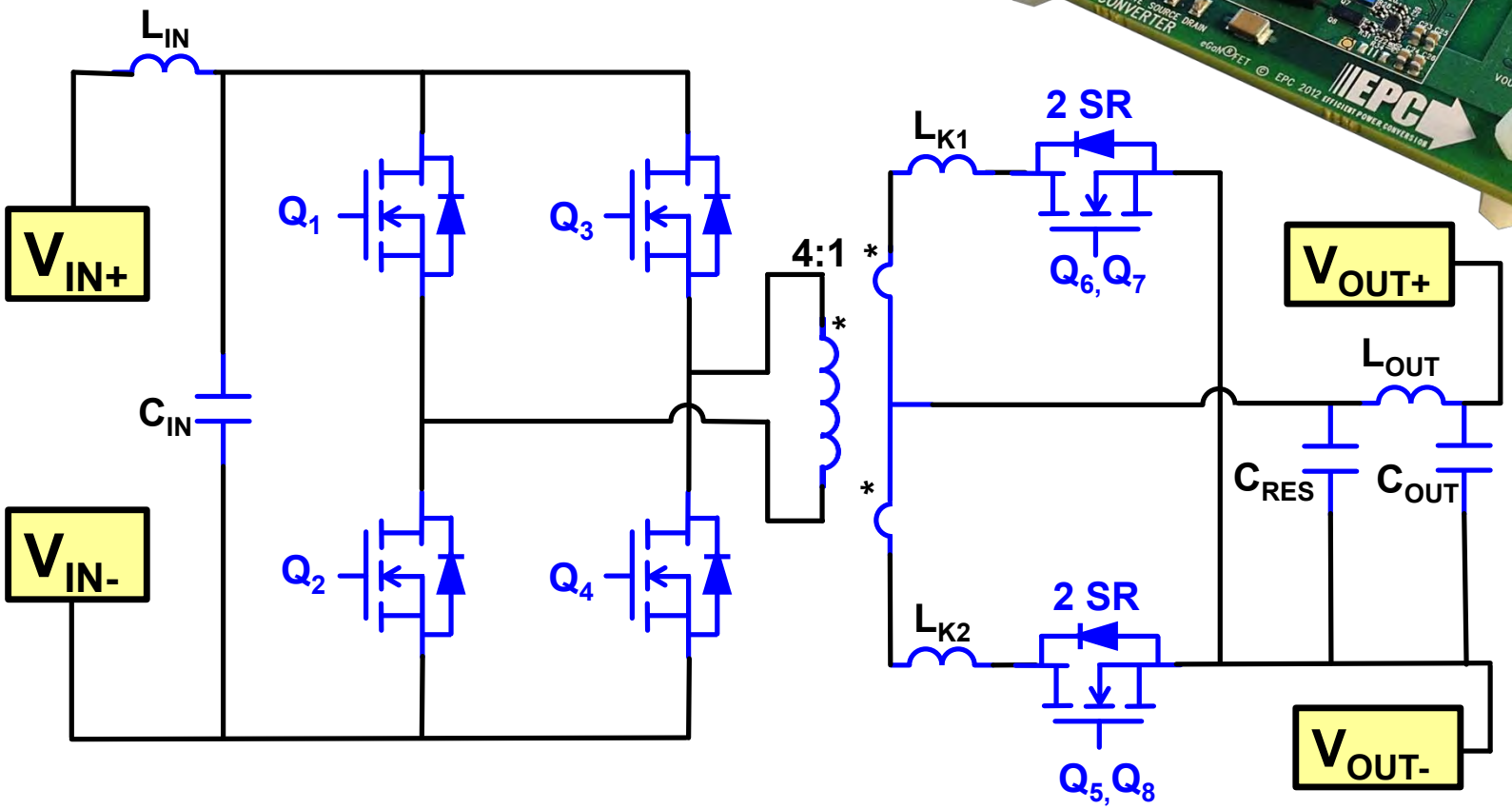
# EPC9105 Bus Converter



## EPC9105 Demonstration Board

**36 - 60 $V_{IN}$, 12 $V_{OUT}$, 350 W, 1.2 MHz**

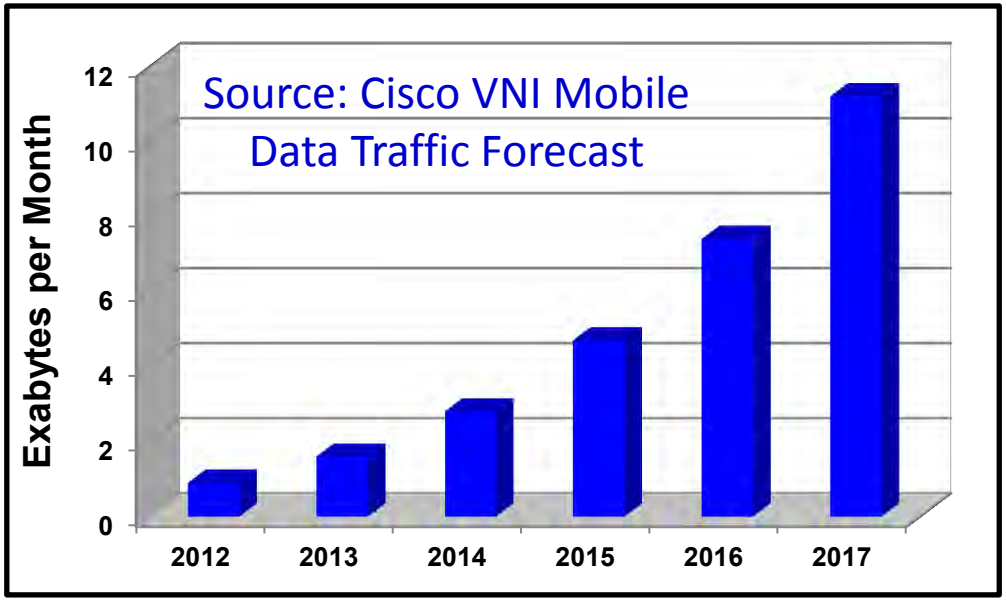


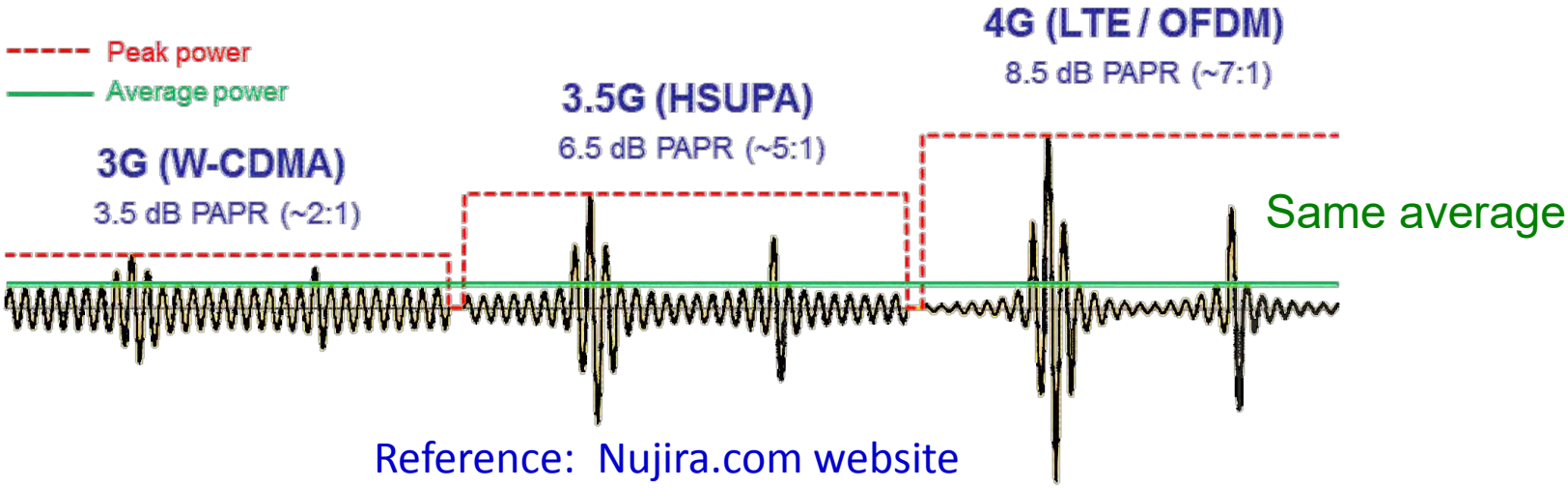
# Envelope Tracking

# Why Envelope Tracking?





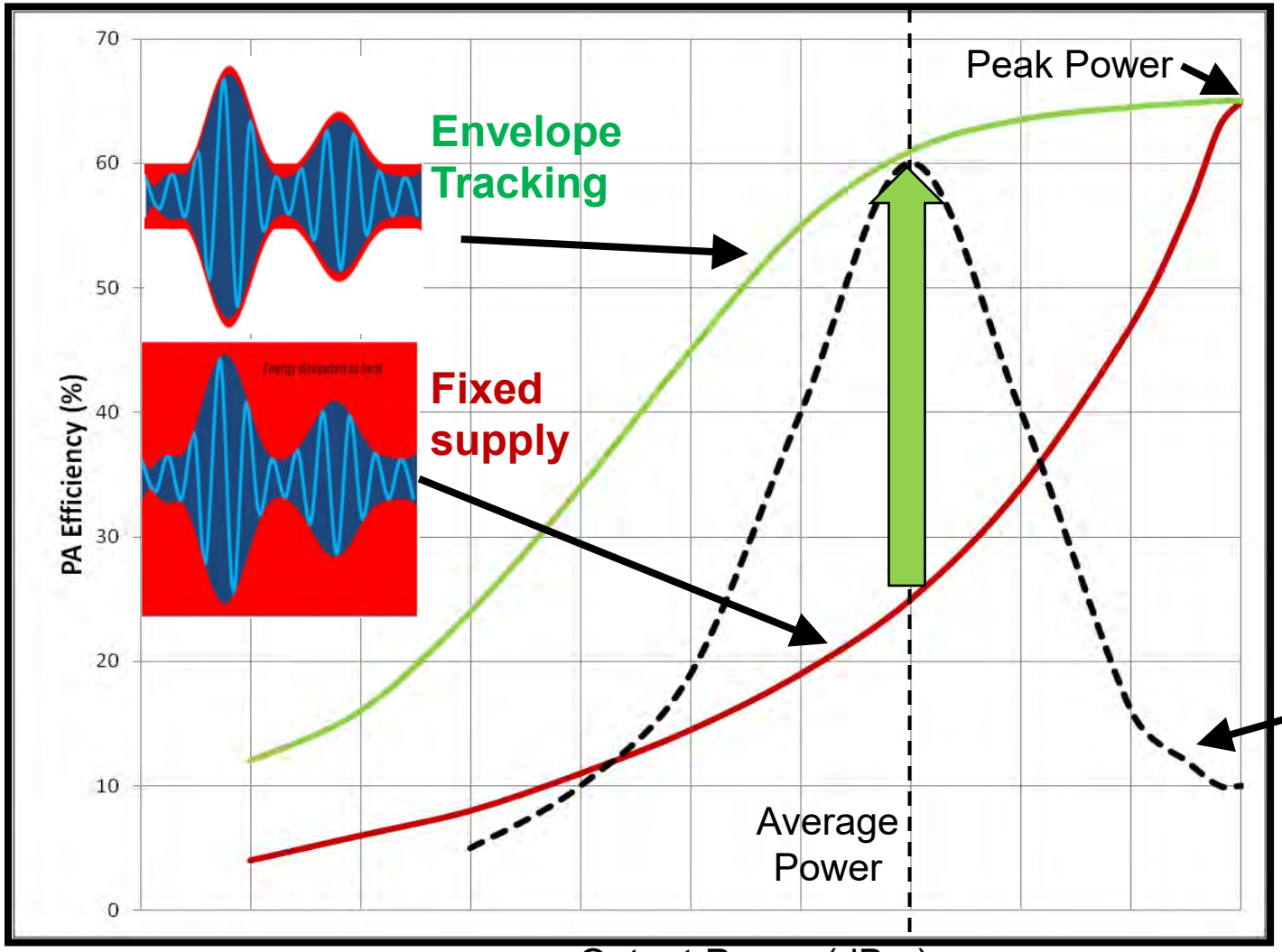

**66% Compound annual growth rate (CAGR)**

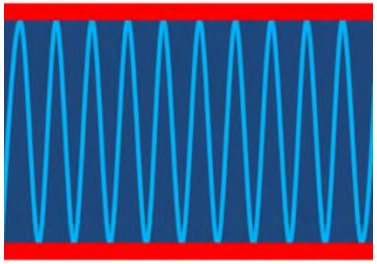



Reference: Nujira.com website

# Envelope Tracking



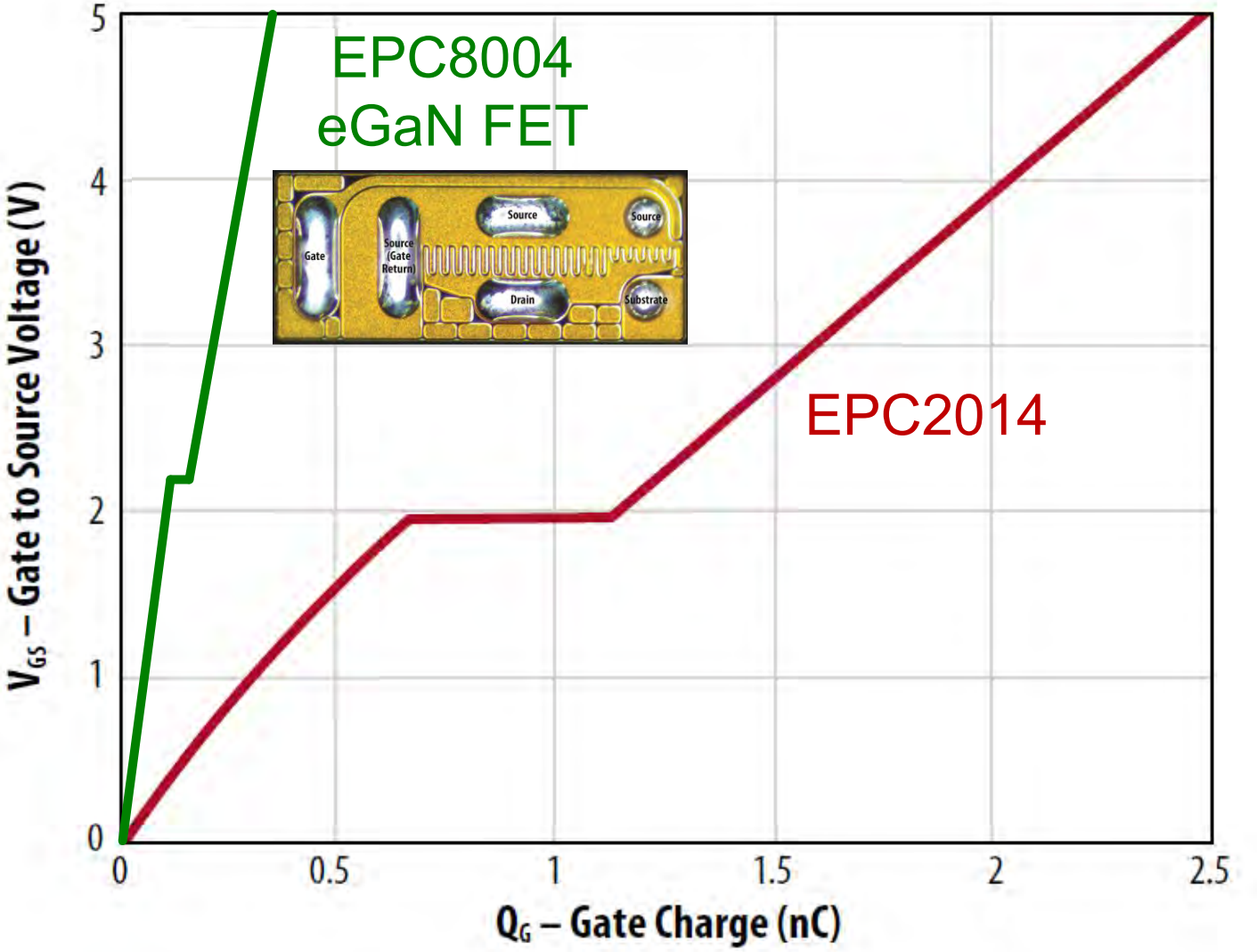


**PAPR = 0dB**
**Peak efficiency up to 65%**

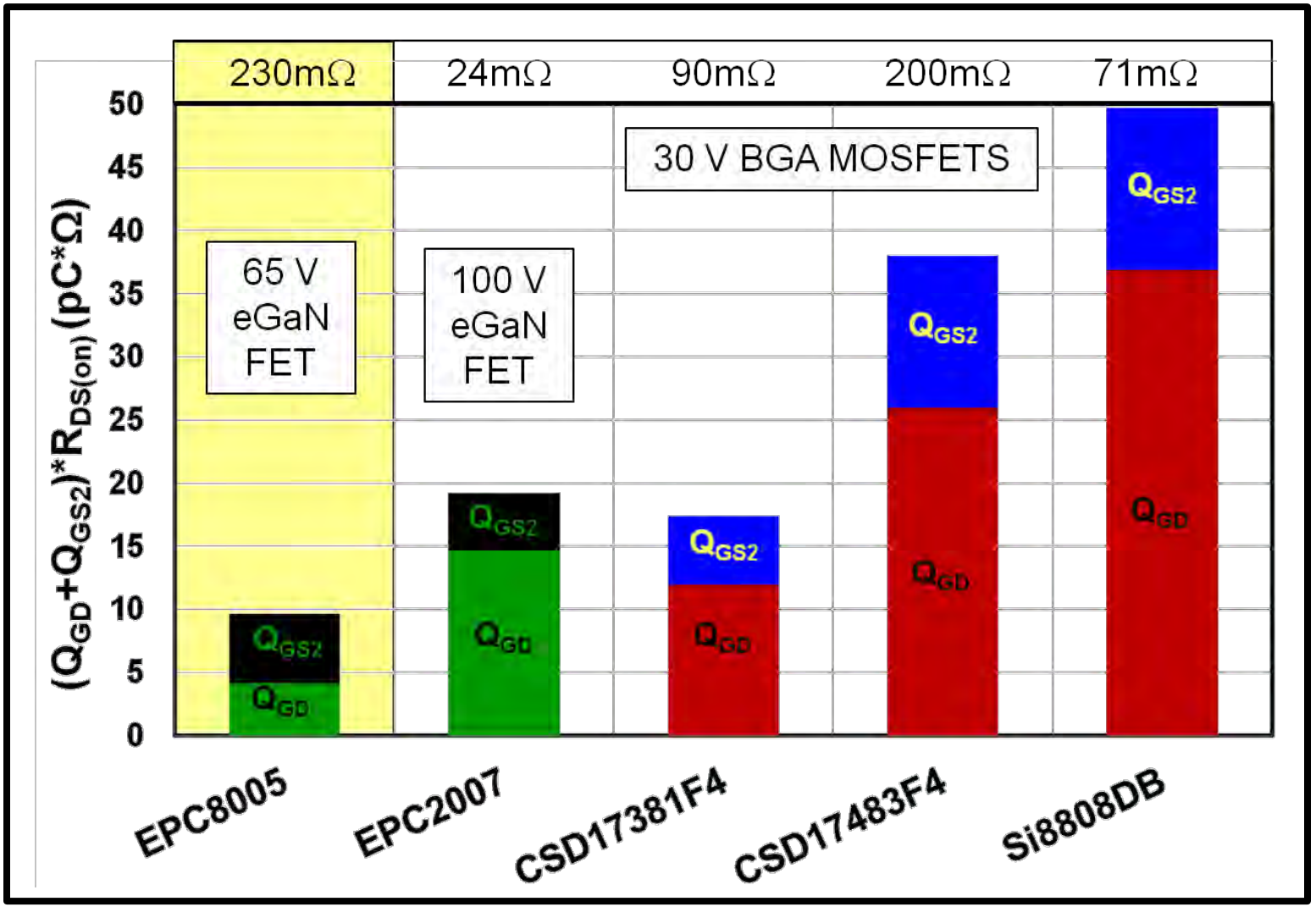
# EPC8000 Series





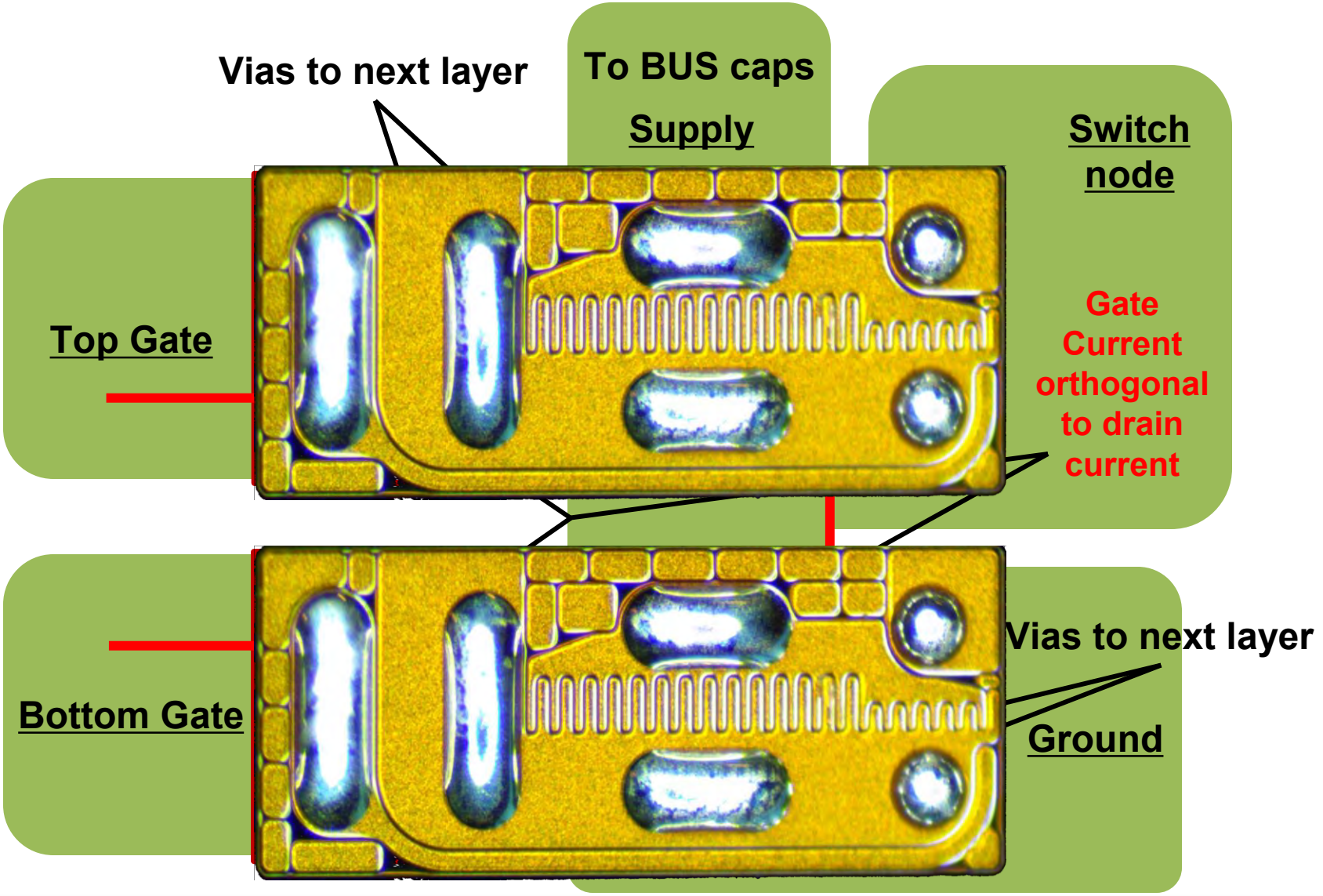
# Hard Switching FOM





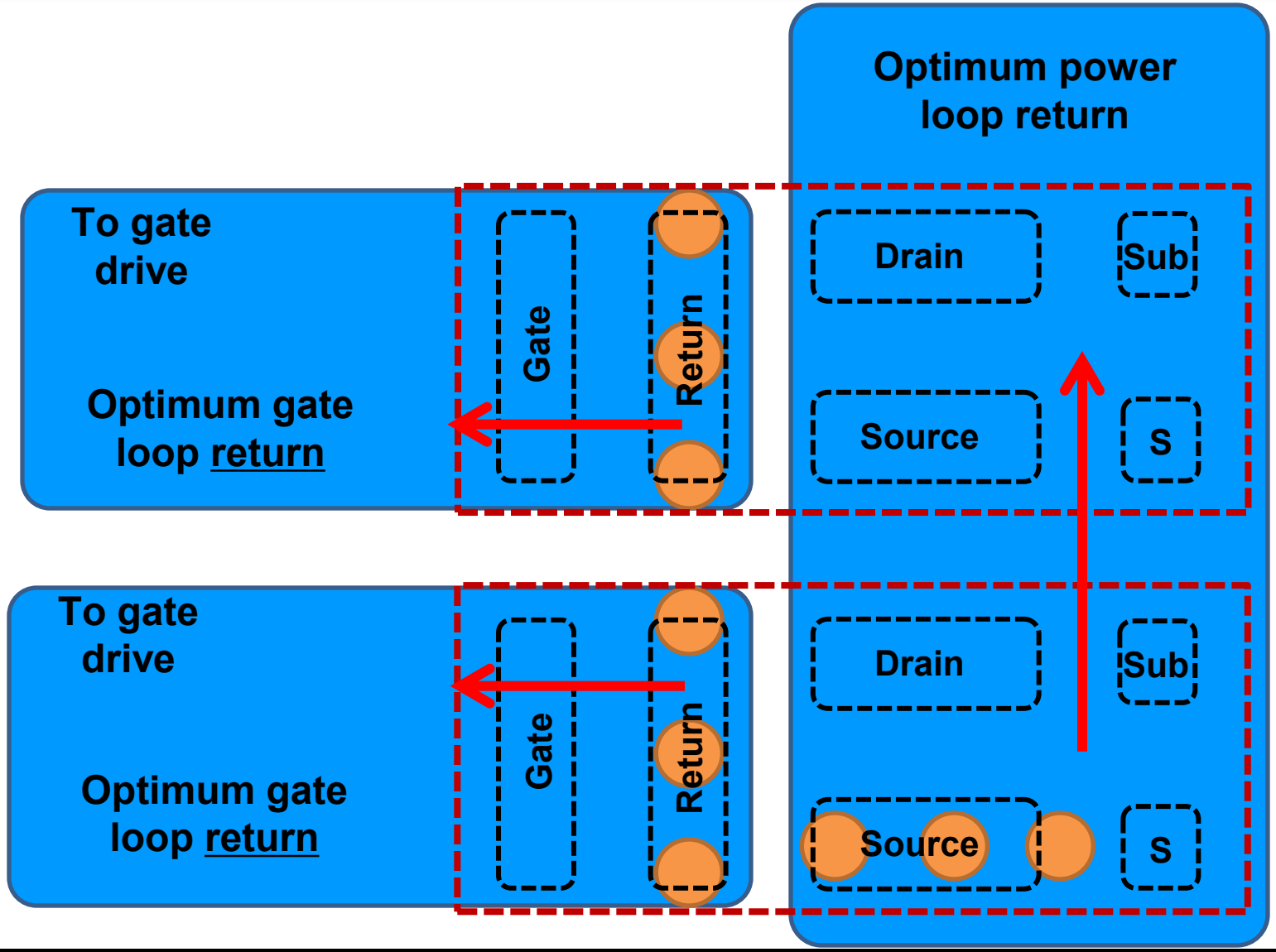
# HB Layout – Top Layer





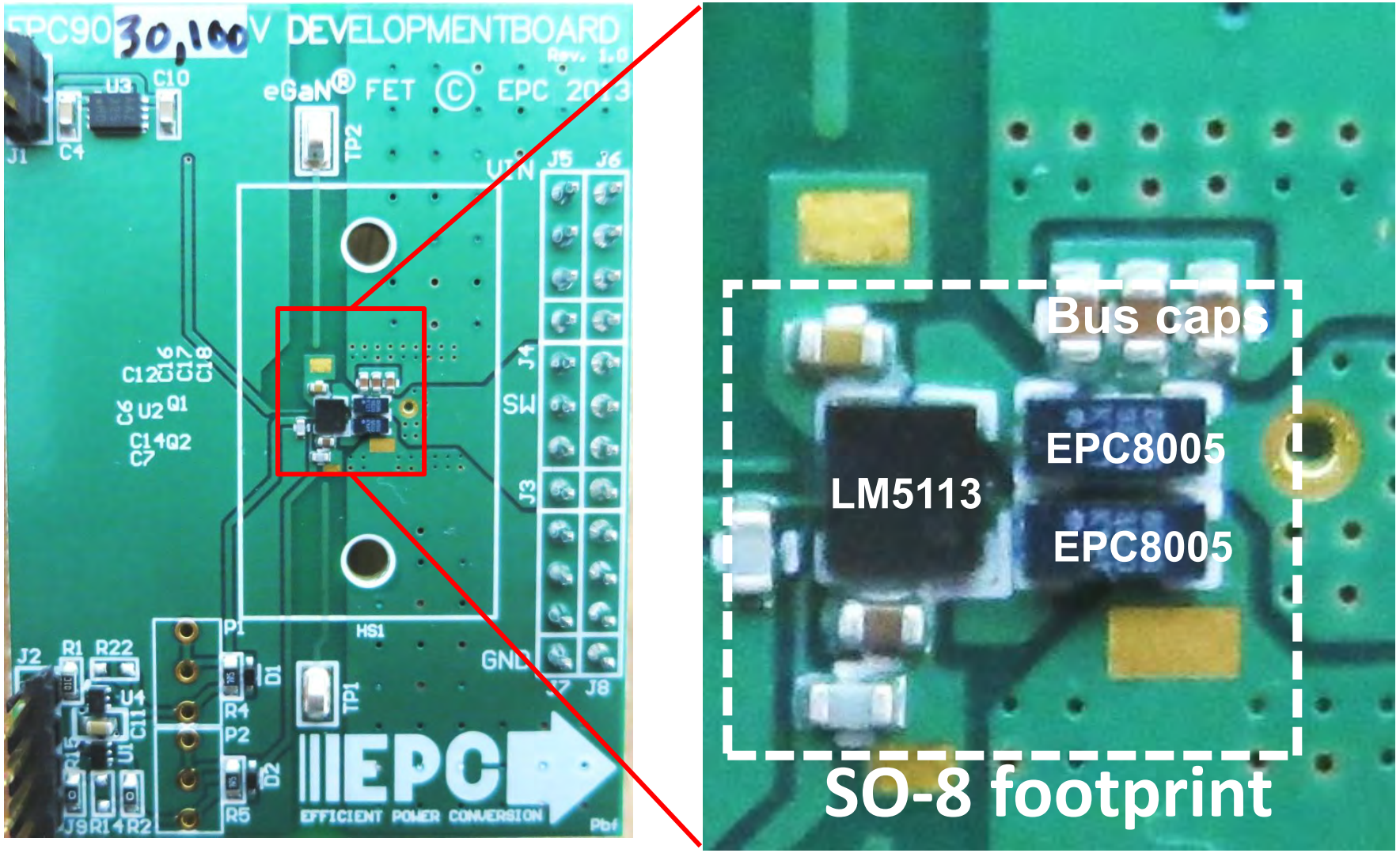
# HB Layout – Inner Layer 1





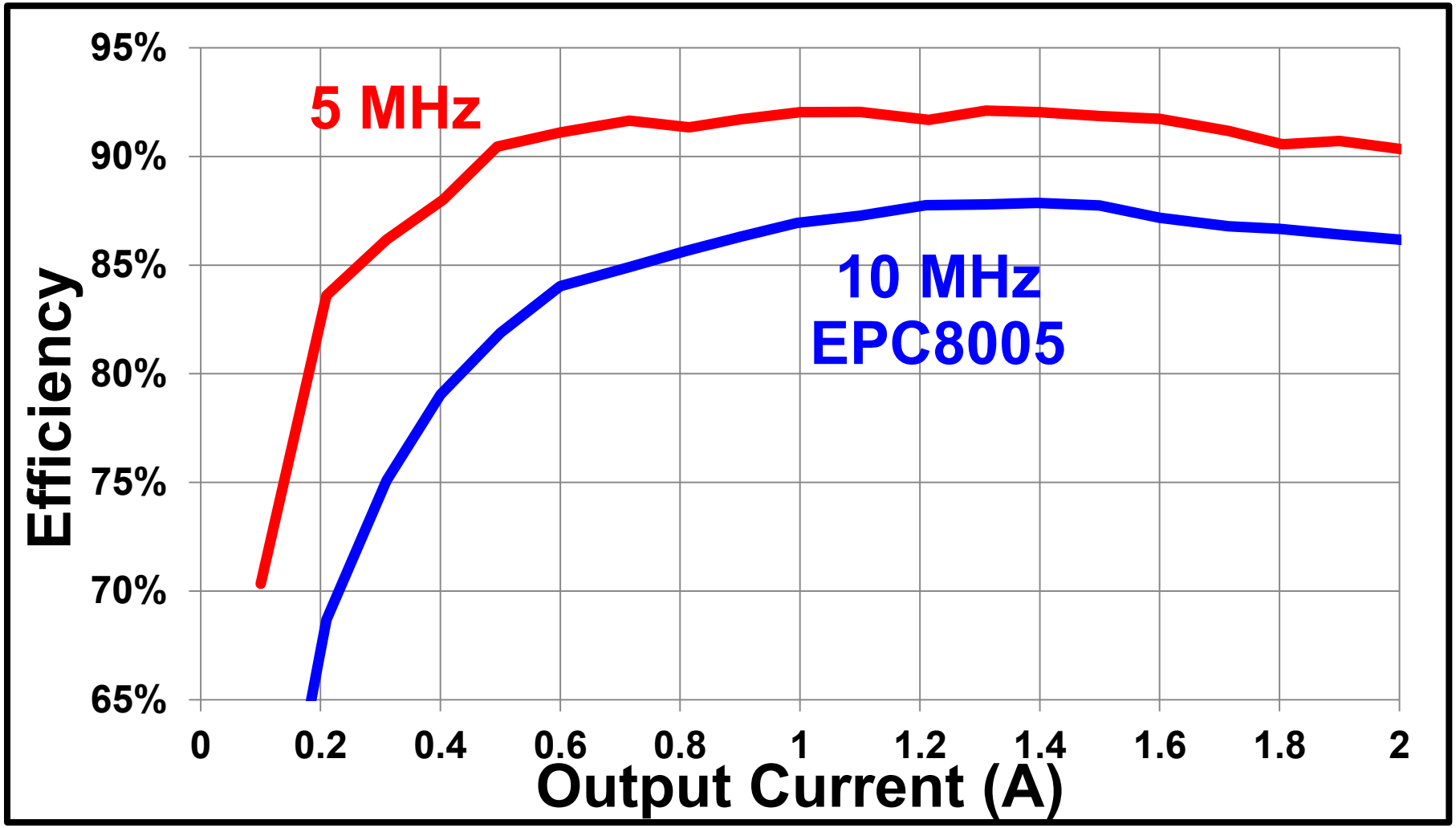
# Envelope Tracking Prototype Board





# High Frequency Efficiency

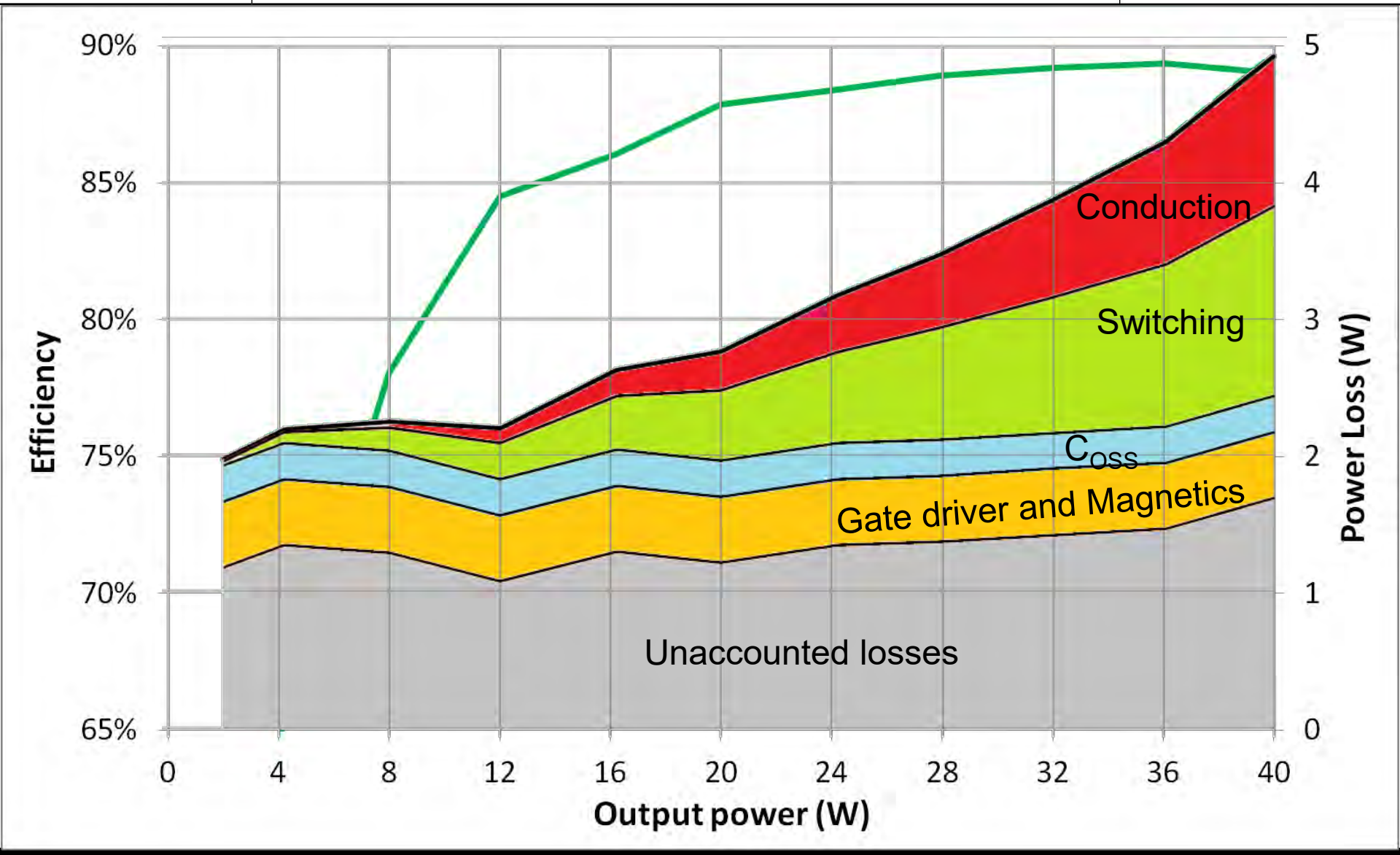




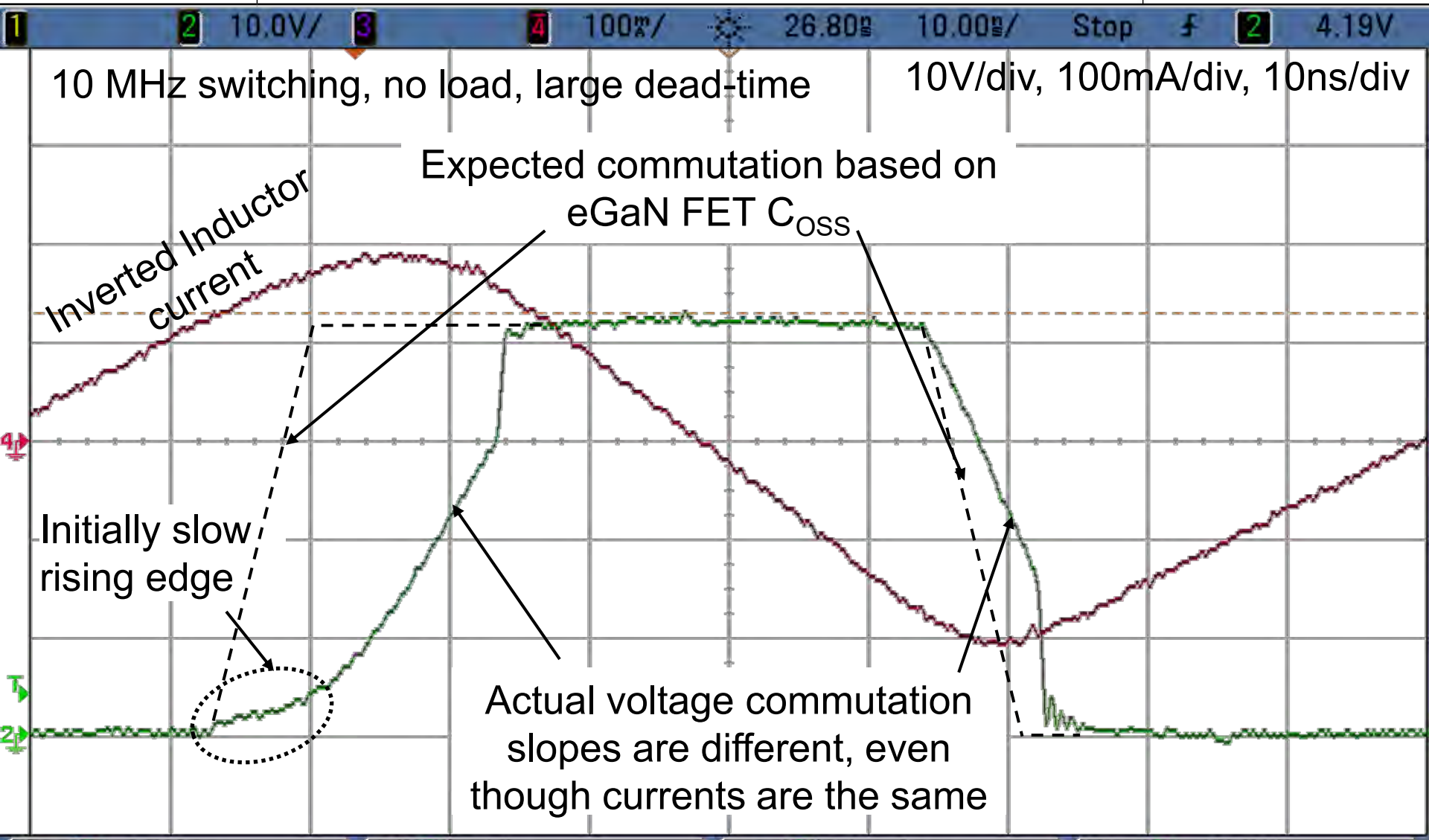

$V_{IN}$=42 V $V_{OUT}$=20 V

# 42$V_{IN}$, 10 MHz Losses



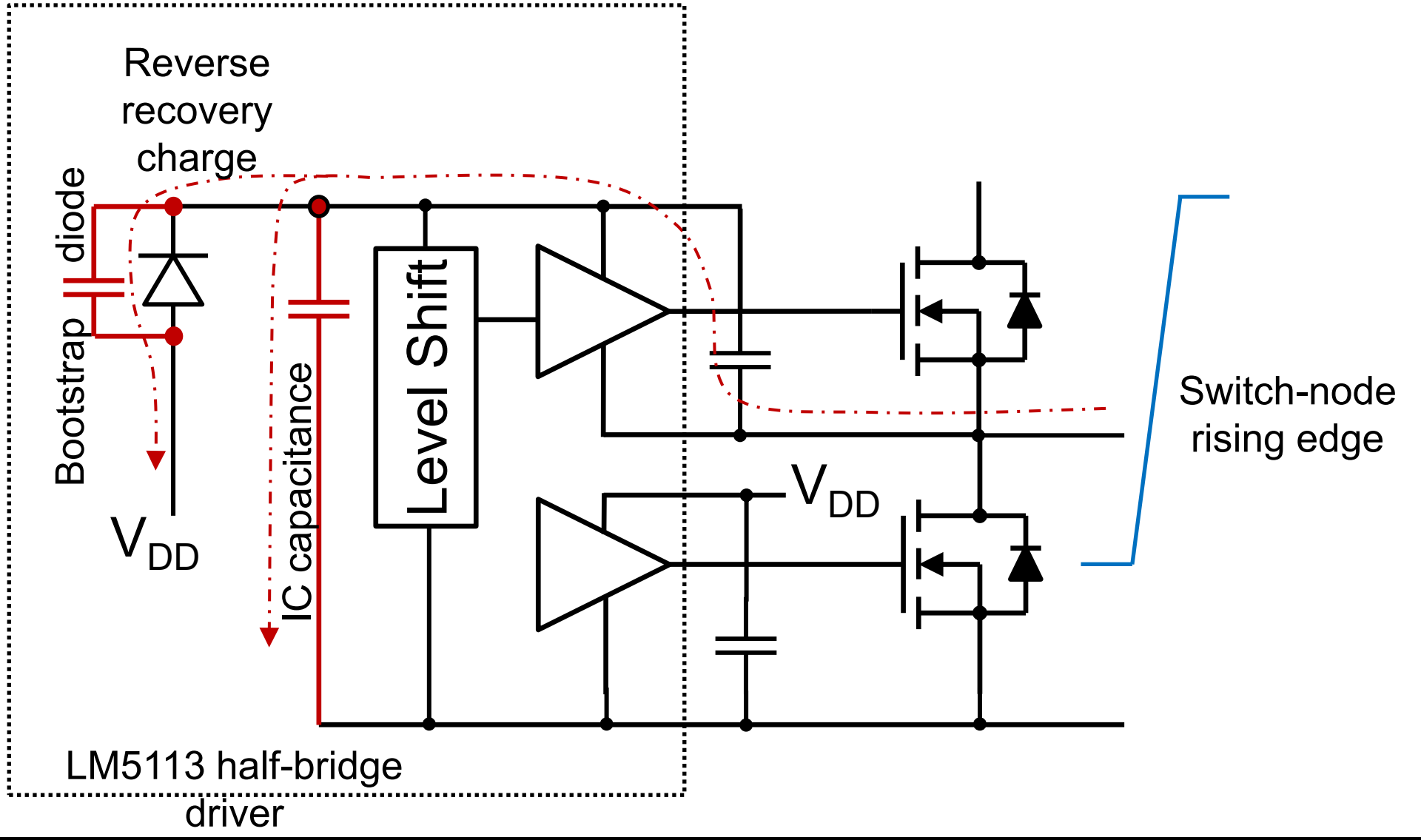


# No-Load Switching

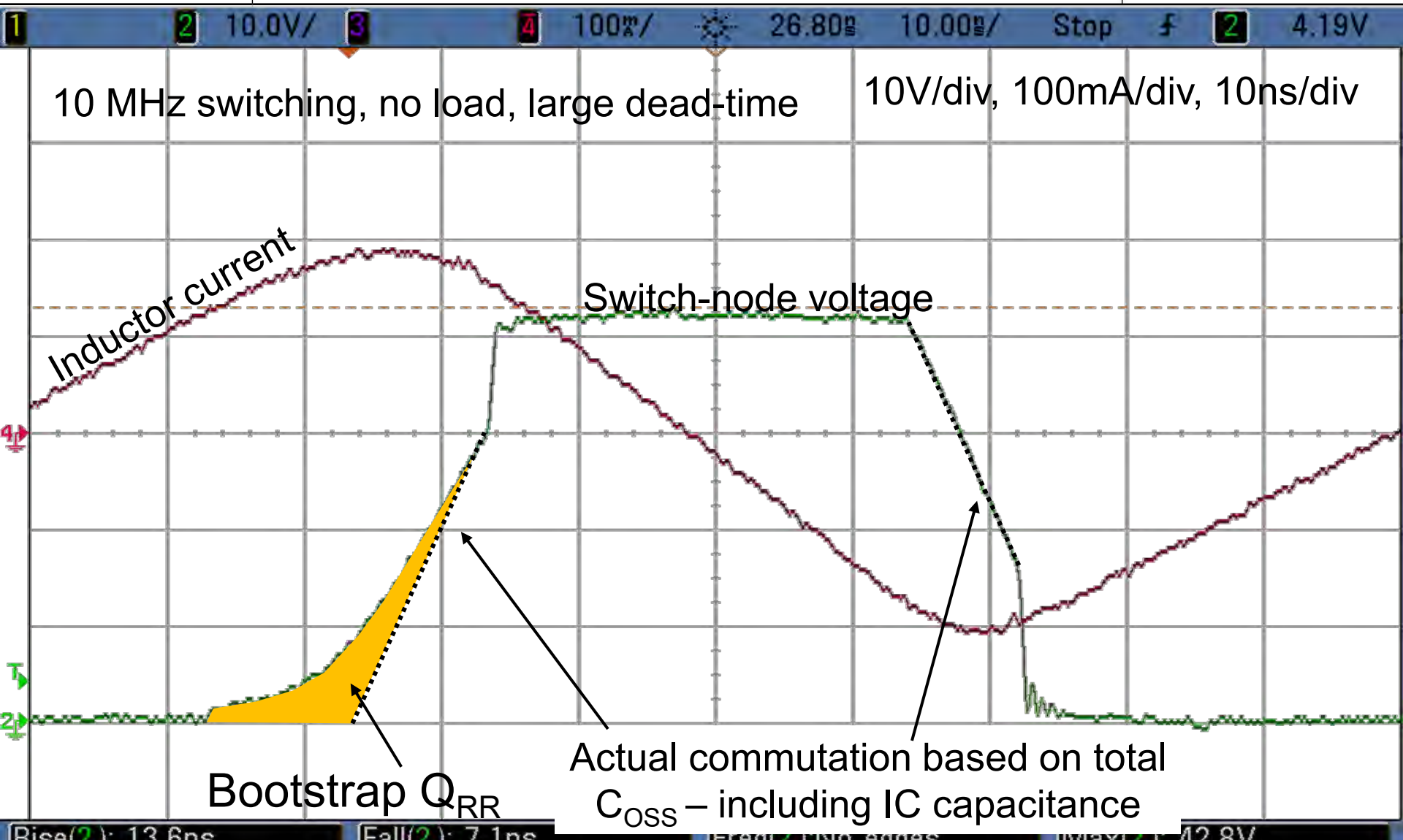


# Parasitic Losses



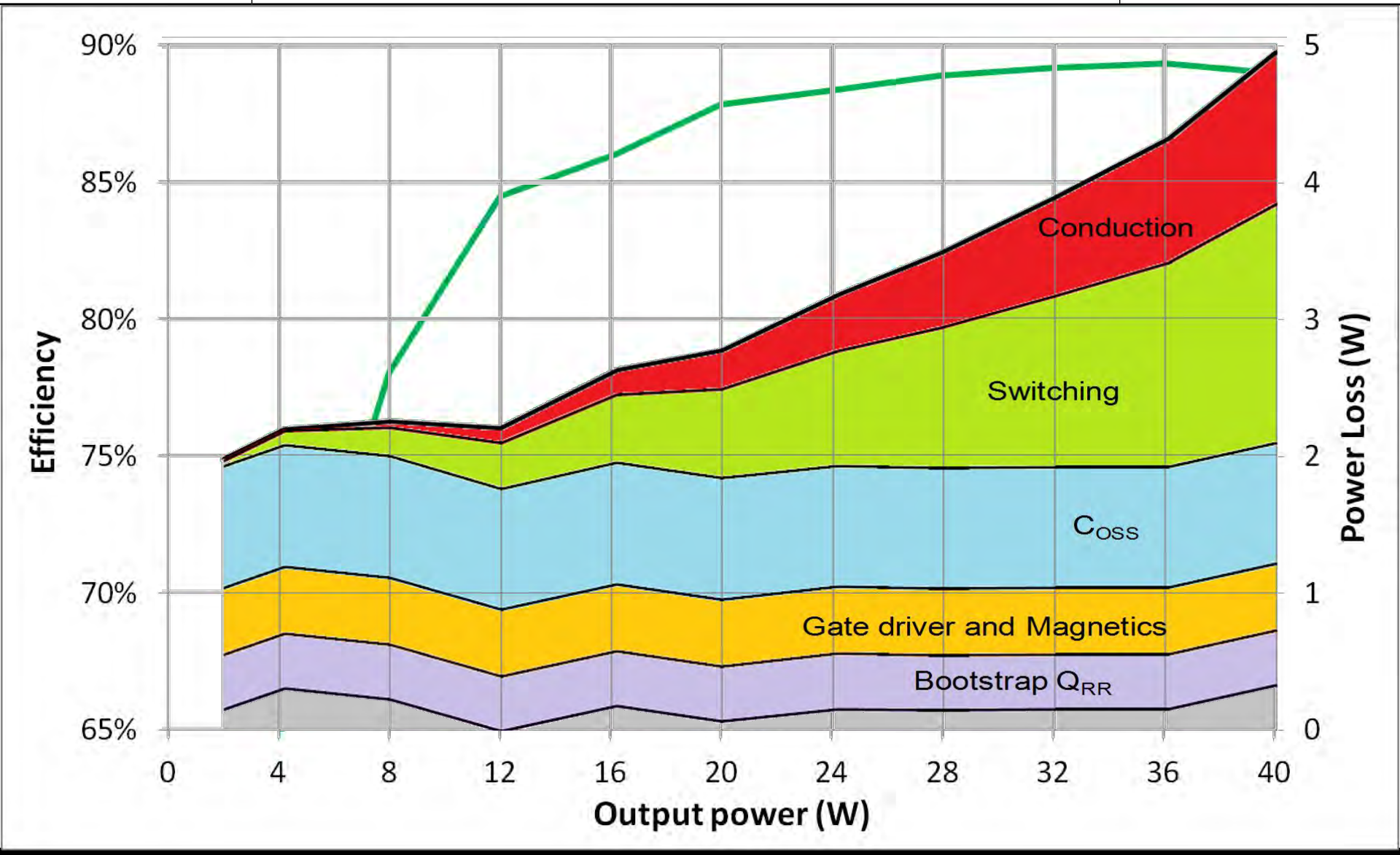


# Loss Breakdown



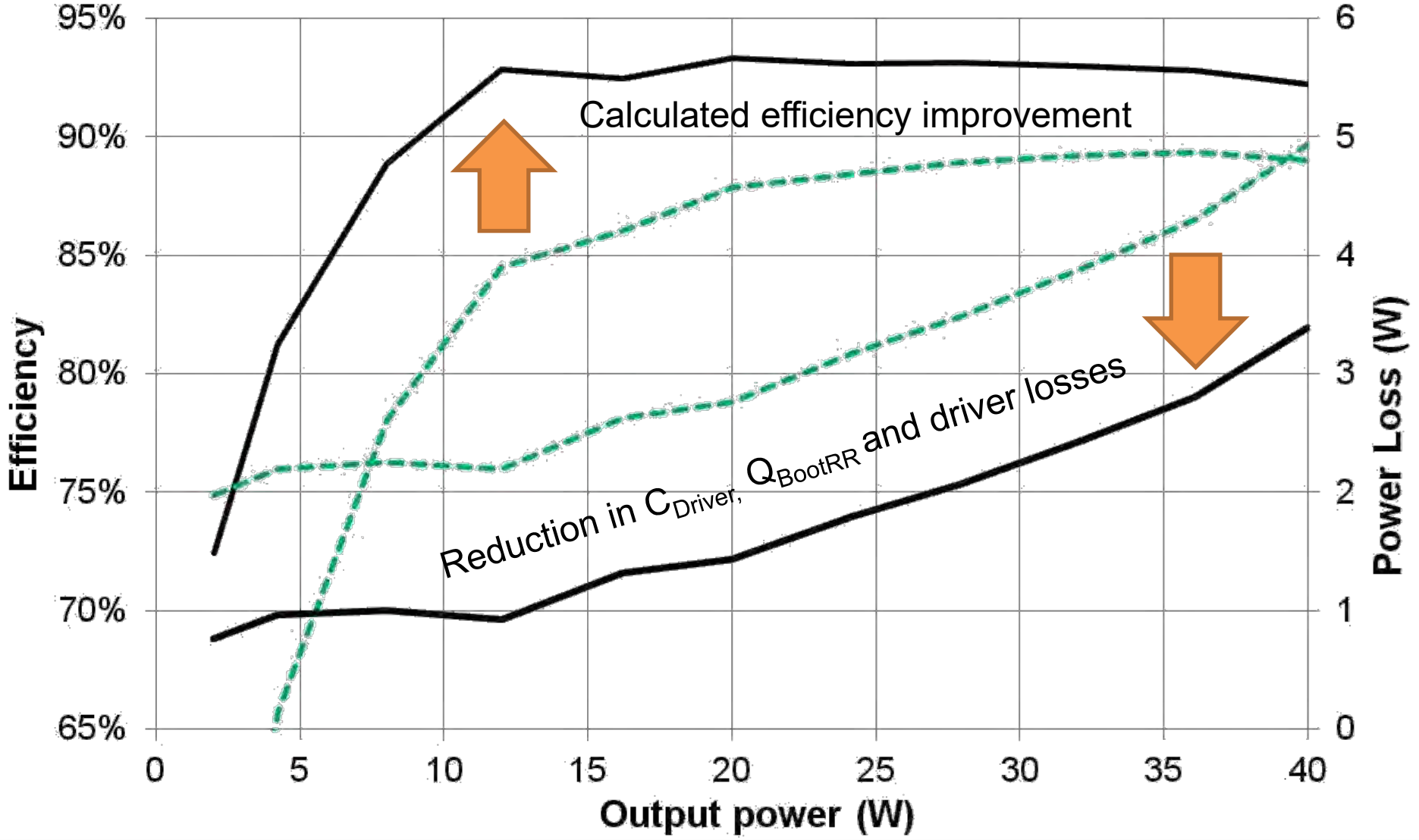
# 42$V_{IN}$, 10 MHz Losses





# eGaN FET Limited Efficiency

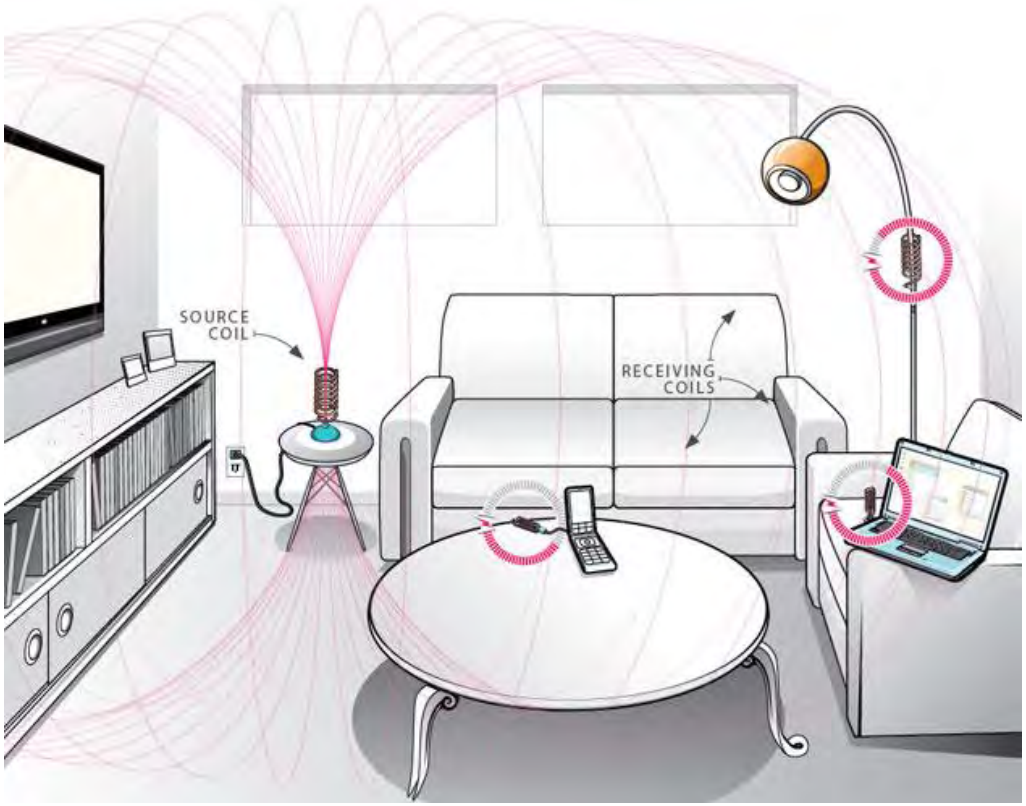




# Wireless Power

# Wireless Power

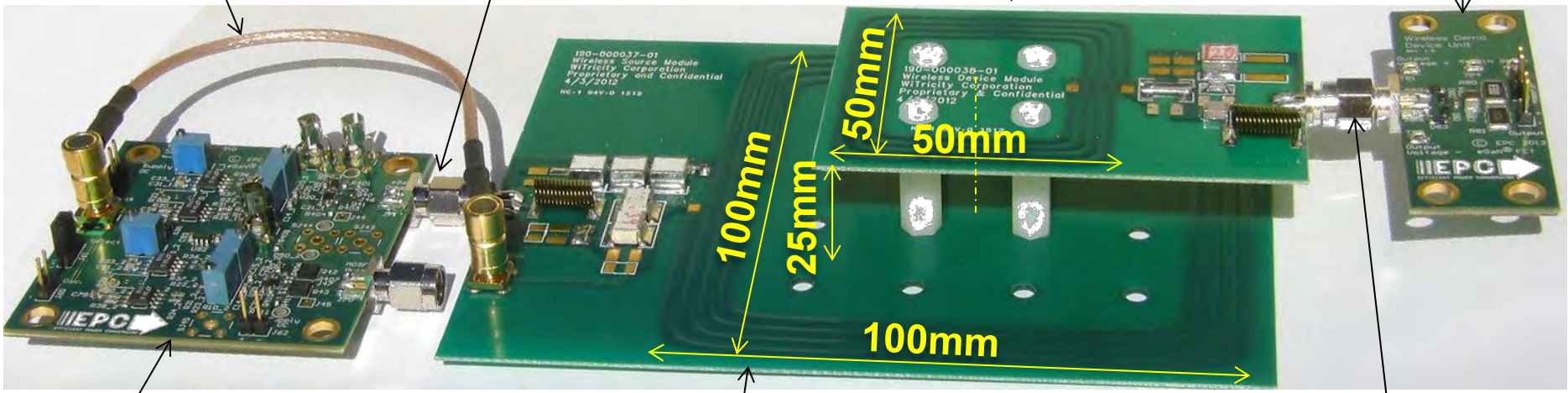





- The global wireless charging market is estimated to grow to $10B by 2018, a CAGR of 42.6%
- eGaN FETs enable higher efficiency and operation at safer frequencies

# Experimental System Setup

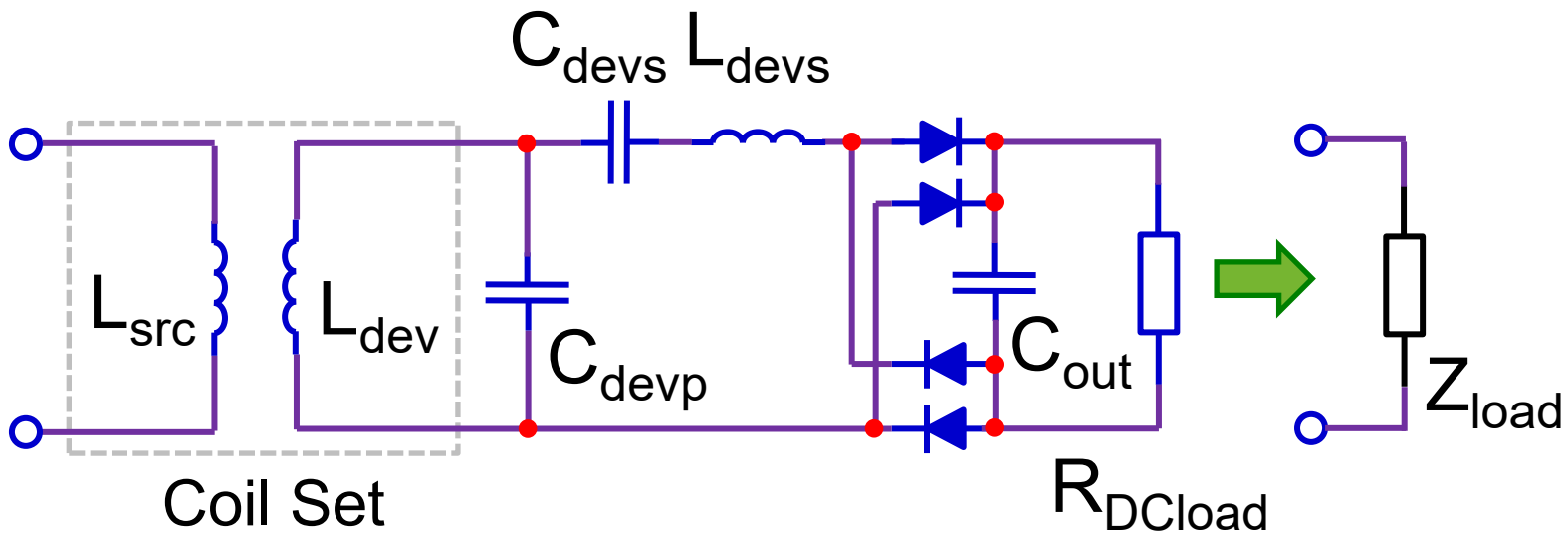




# Coil Simplification



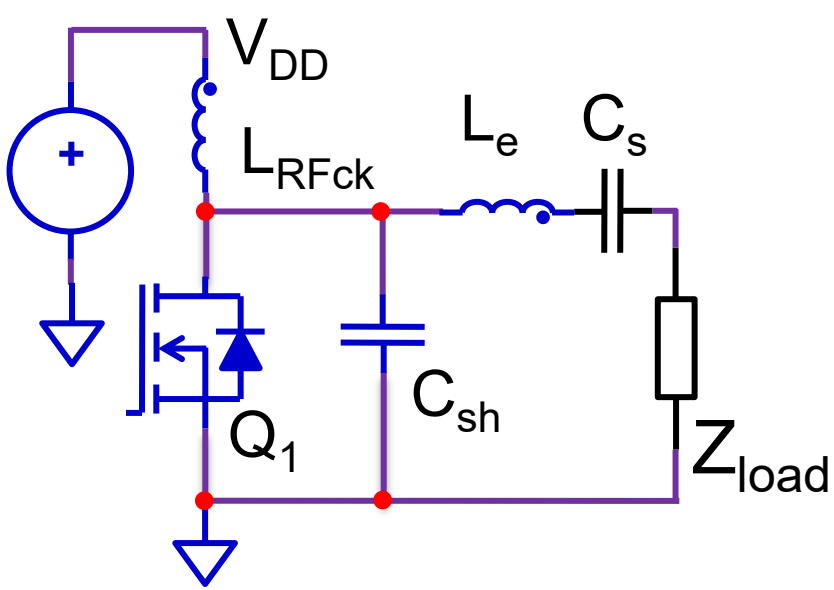
Simplified representation of coil-set for easy comparison between topologies

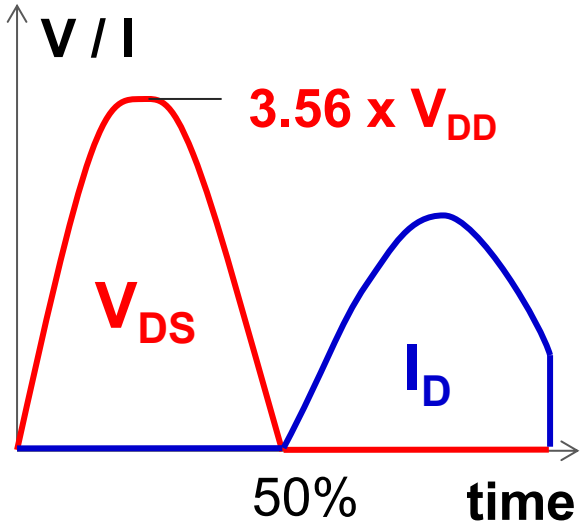


# Single Ended Class-E



- Switch voltage rating ≥ 3.56·Supply ($V_{DD}$).
- $C_{OSS}$ "absorbed" into matching network.
- Susceptible to load variation - high FET losses.
- Coil voltage ≈ 0.707·$V_{DD}$ [$V_{RMS}$].

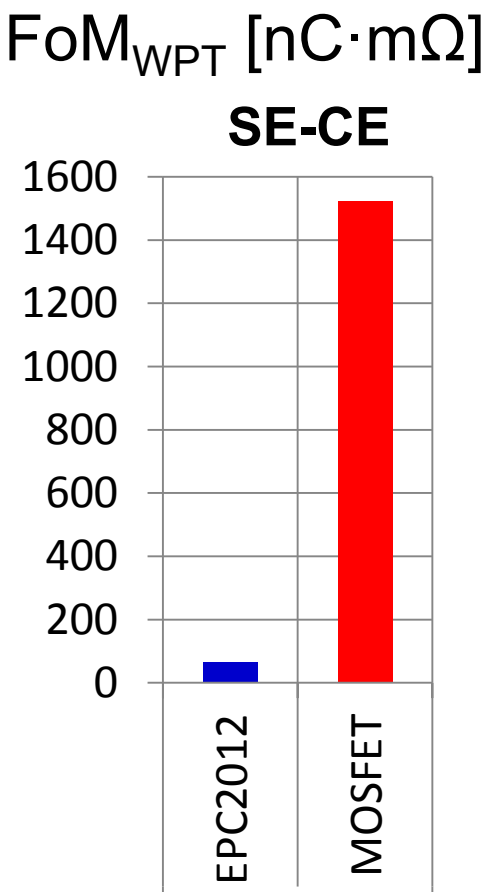


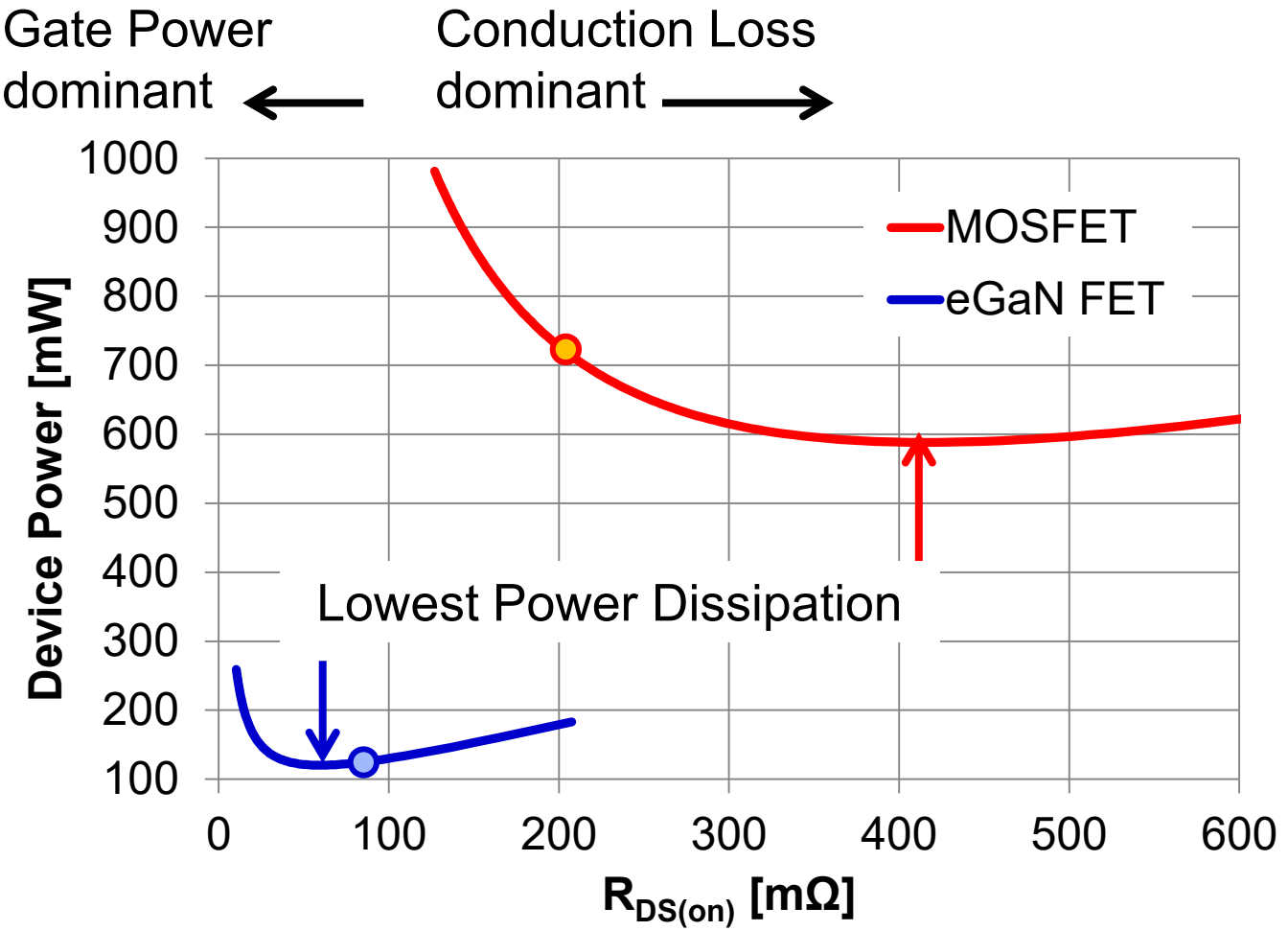




Ideal Waveforms

# Class-E Device Comparison





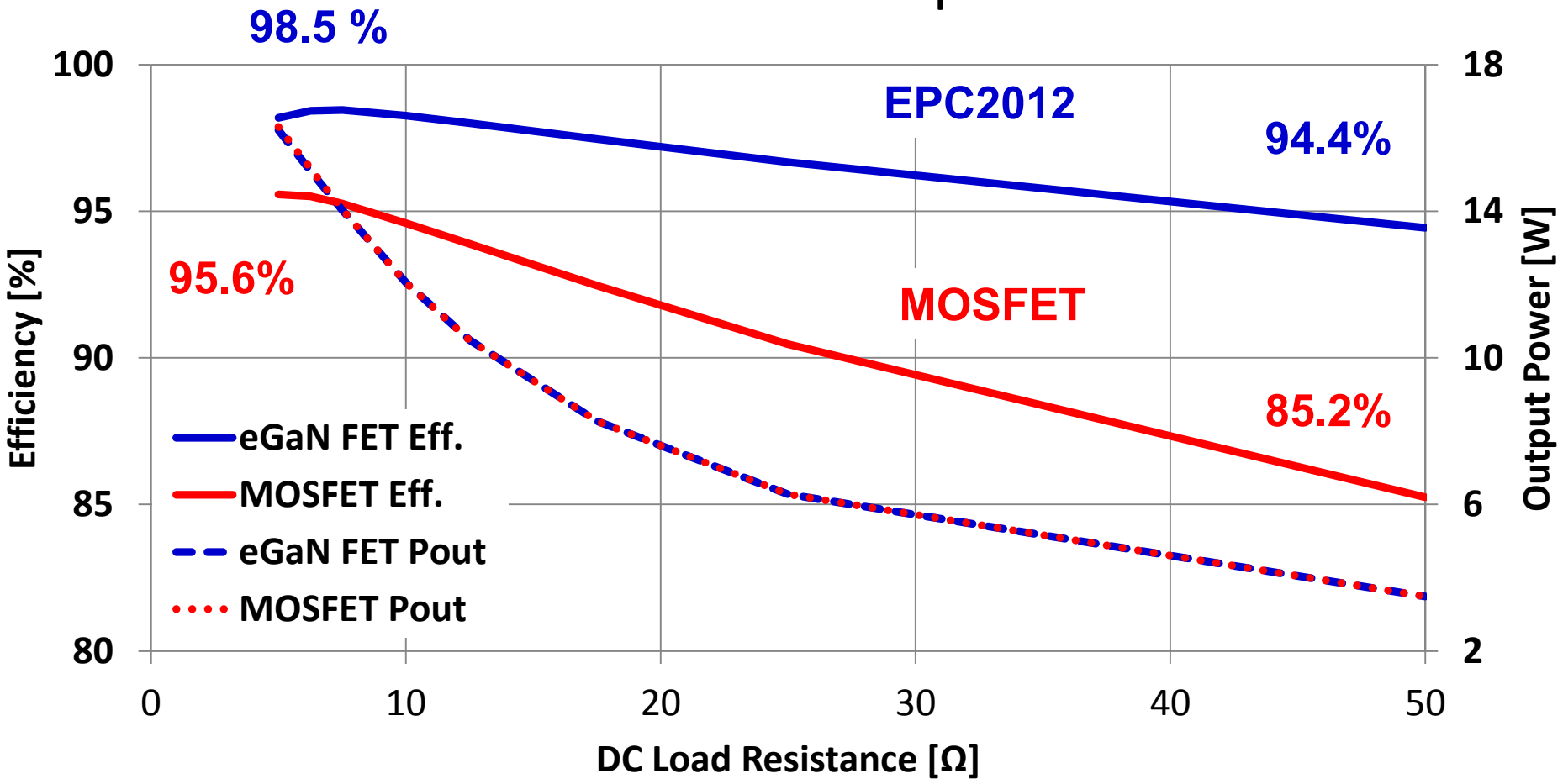




$$FOM_{WPT} = R_{DS(on)} \cdot (Q_G - Q_{GD})$$

# Class-E Analysis Comparison

Peak Power Device losses = 279 mW

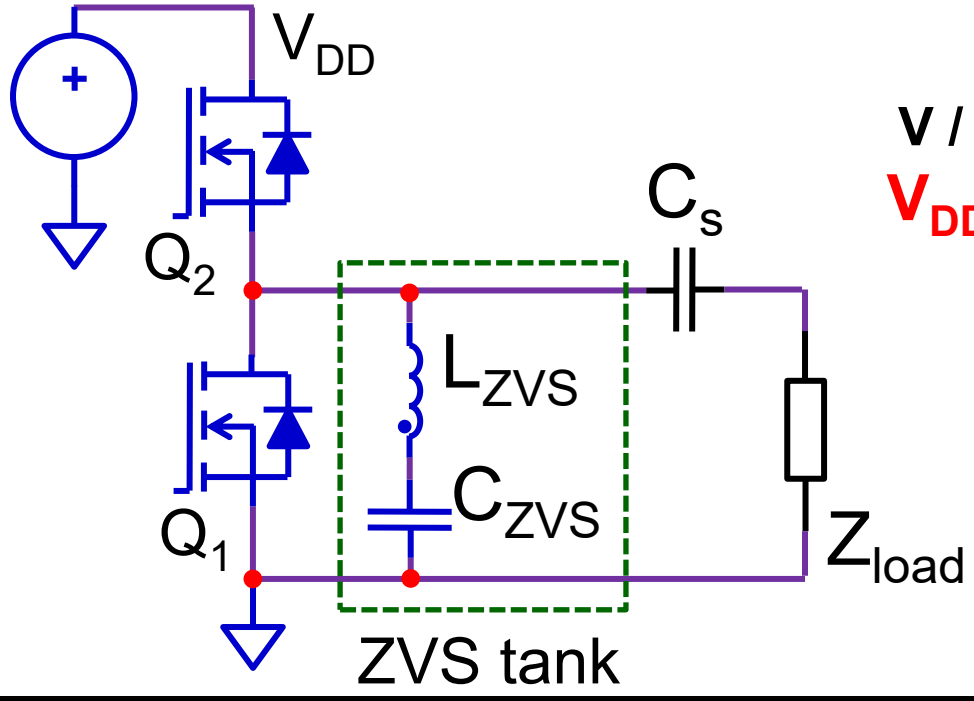
No Heat-Sink Required

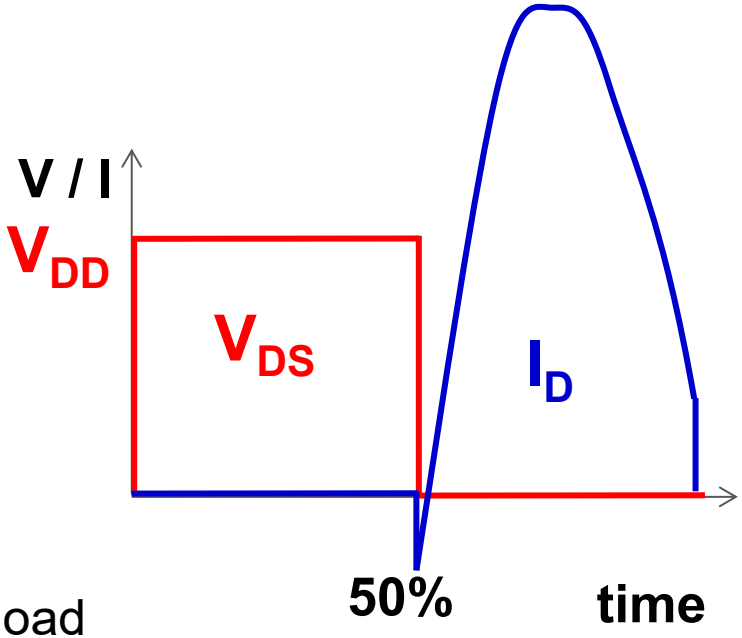


# ZVS Class-D



- Switch voltage rating = Supply ($V_{DD}$).
- $C_{OSS}$ voltage is transitioned by the ZVS tank .
- ZVS tank circuit does not carry load current.
- Coil voltage = ½·$V_{DD}$ [$V_{RMS}$].

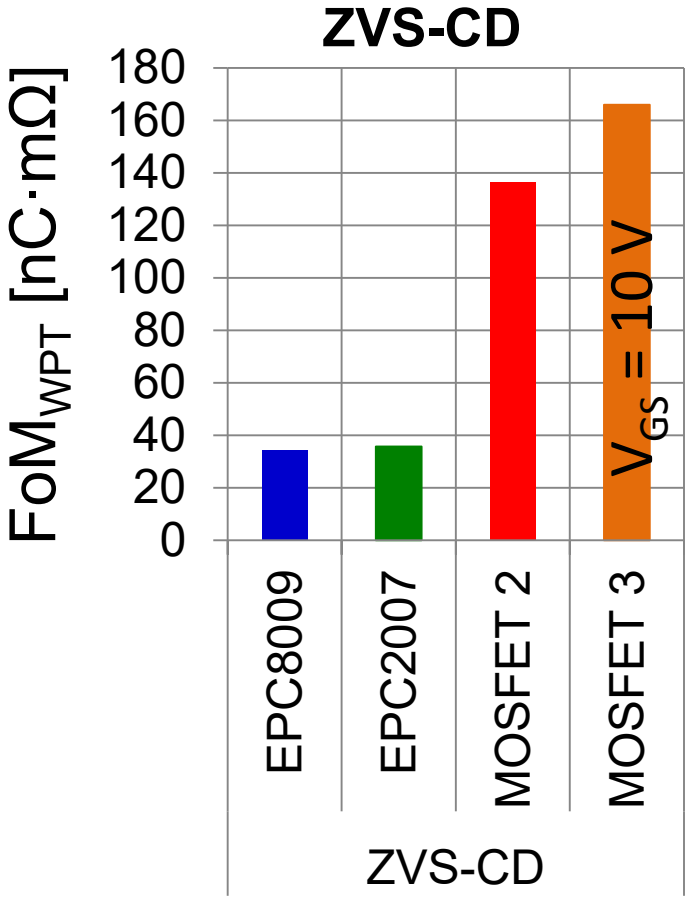



Ideal Waveforms

# Device Comparison

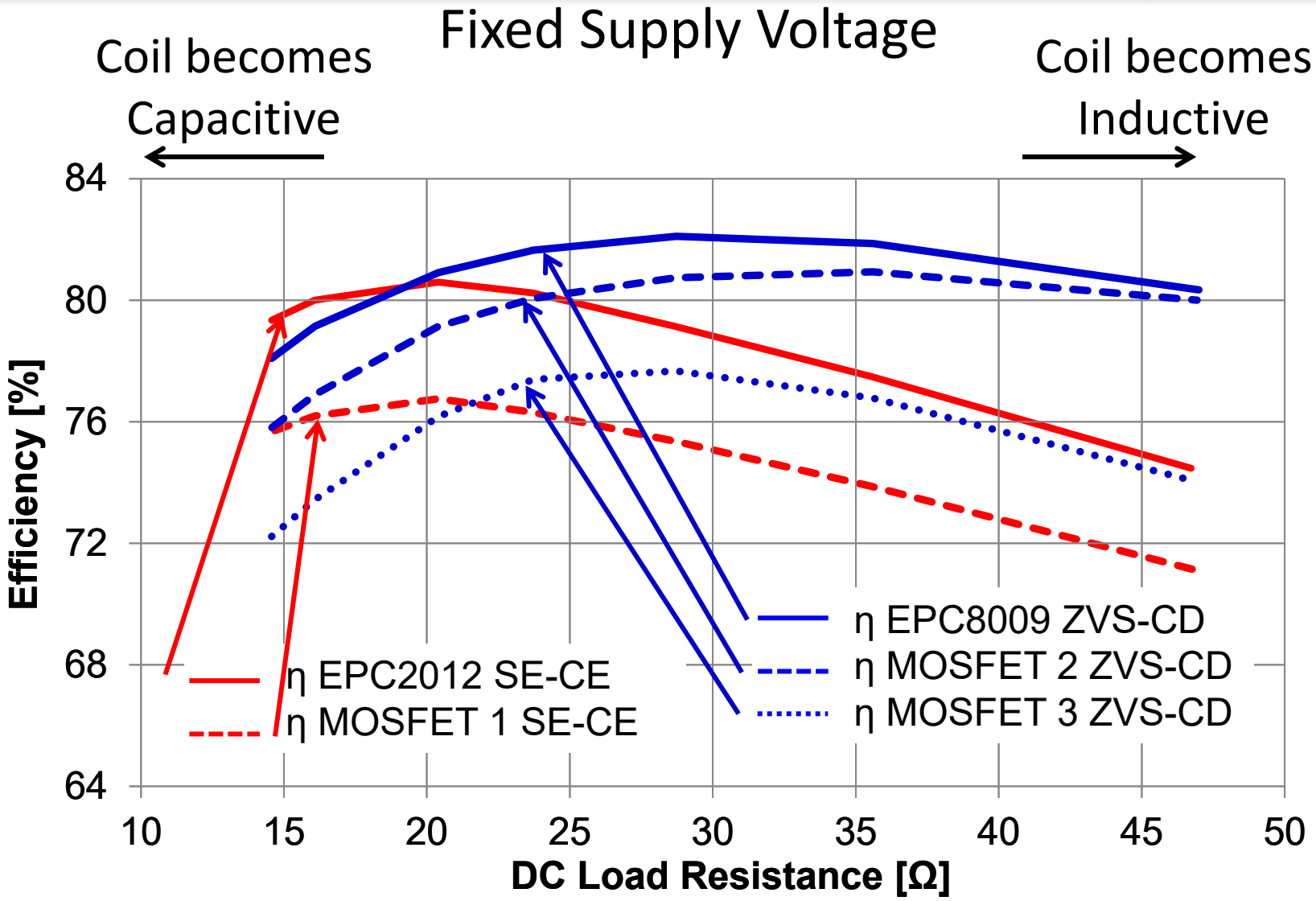





$$FOM_{WPT} = R_{DS(on)} \cdot (Q_G - Q_{GD})$$

# Load Variation Results



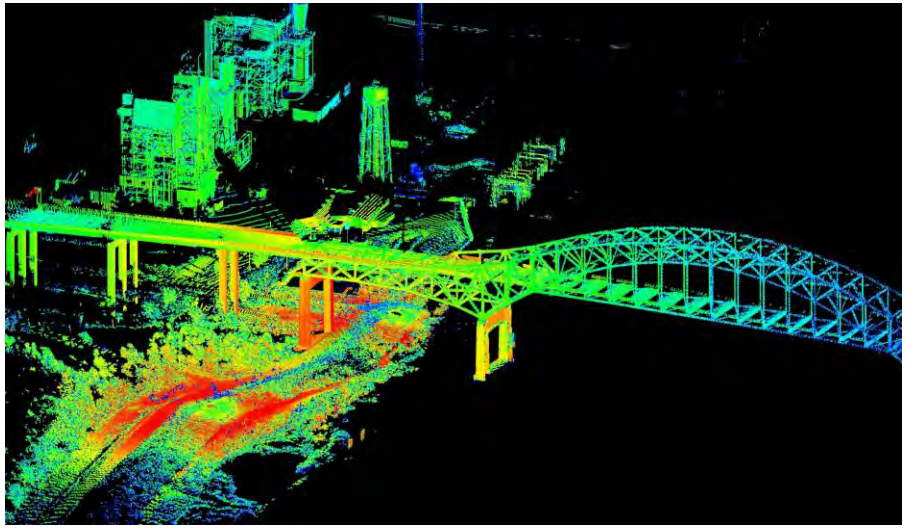


# LiDAR

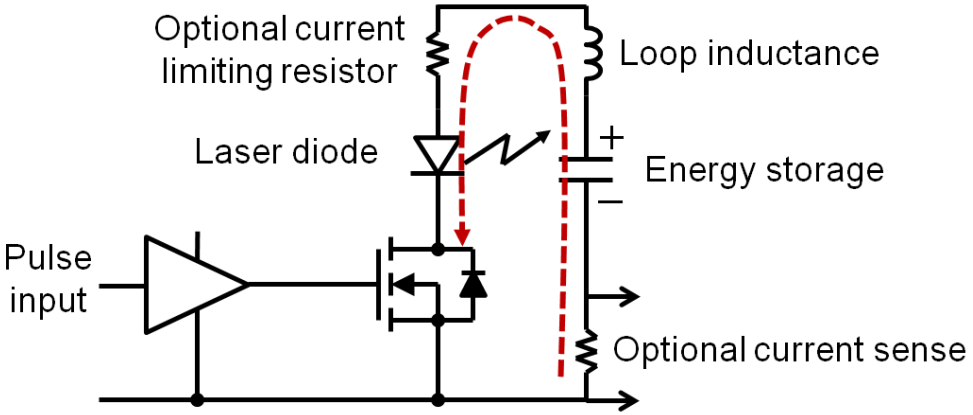
# LIght Detection And Ranging



- Autonomous vehicles
- Video games
- Geology
- Agriculture

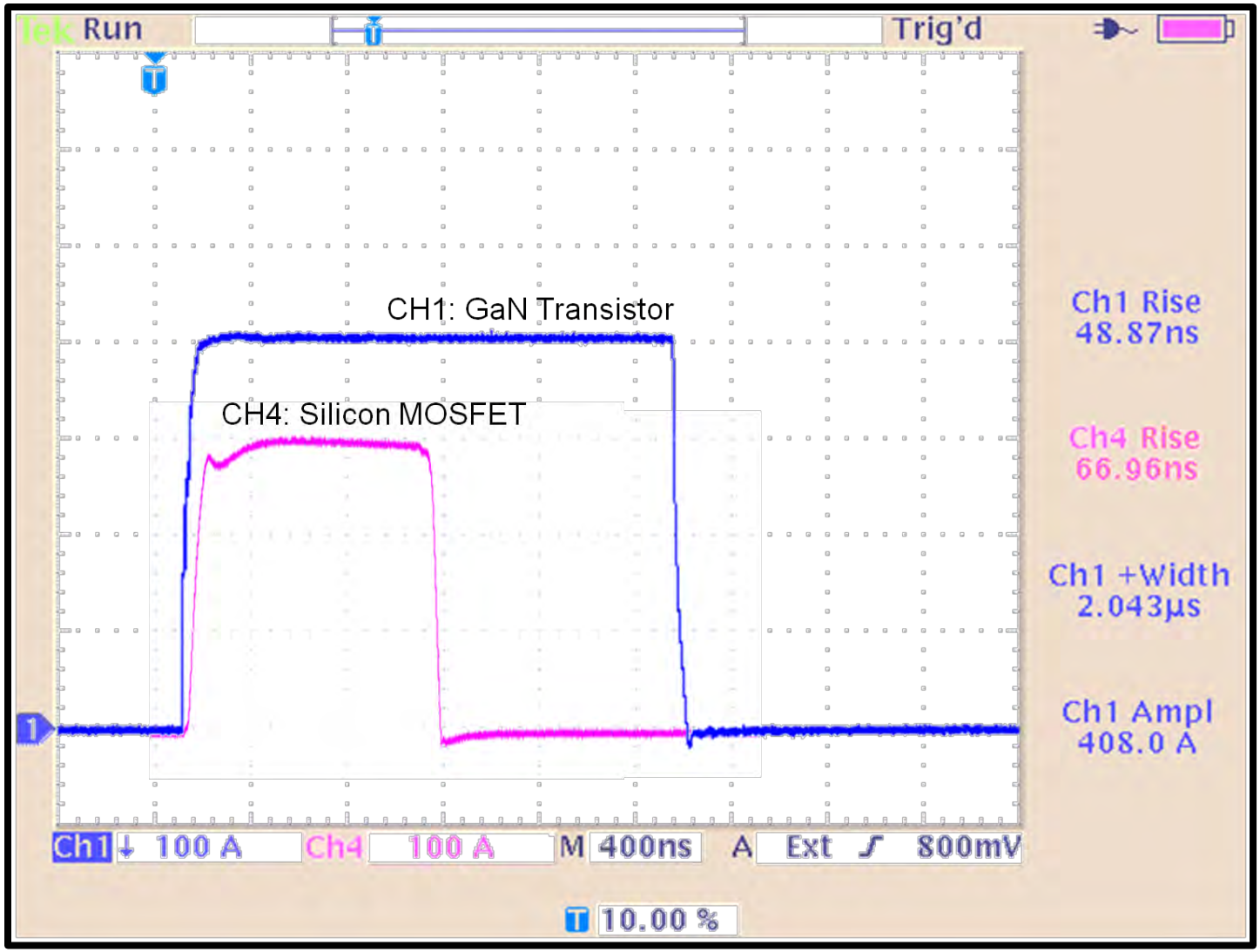


http://www.usgs.gov/blogs/features/usgs_top_story/hurricane-season-is-here/



# LiDAR





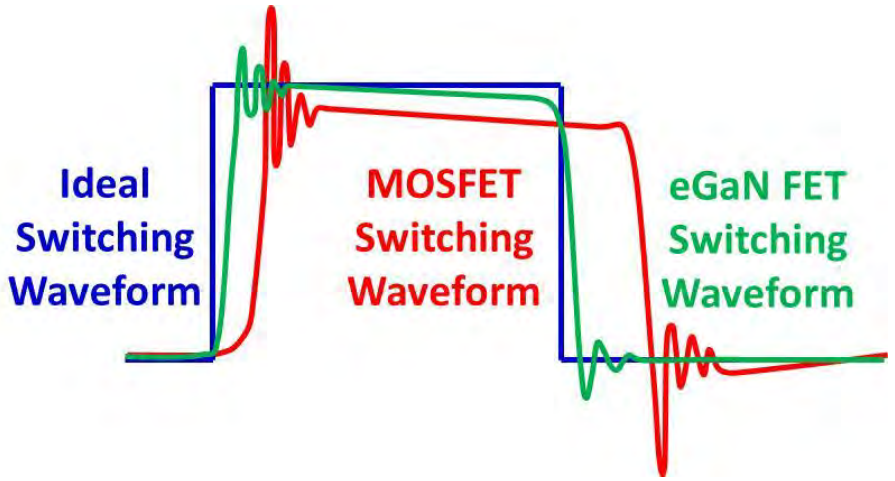

Courtesy of OmniPulse

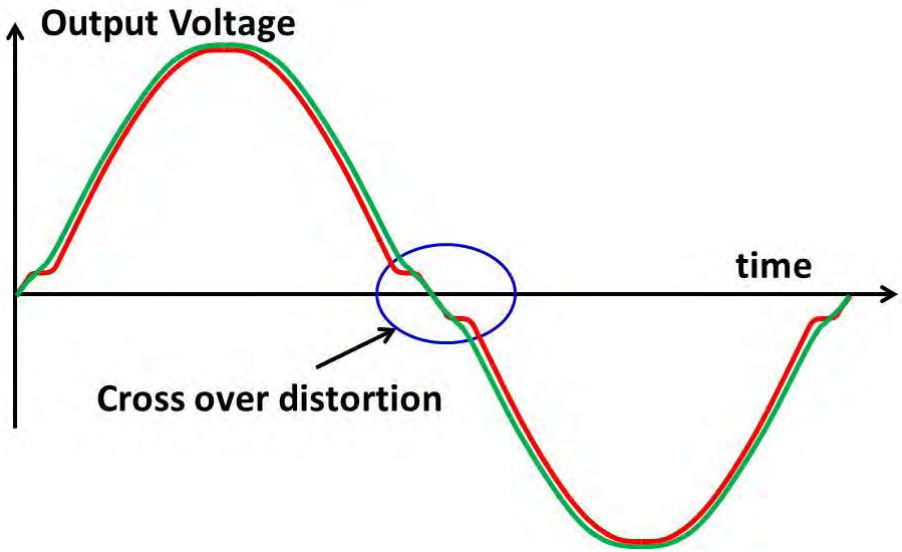
# Class-D Audio

# Why eGaN FETs in Class-D Audio



- Low $R_{DS(on)}$ & Low $C_{OSS}$
  - + High Efficiency
  - + High Damping Factor = Low open loop output Impedance = **Low T-IMD**
- Fast Switching & No Reverse Recovery ($Q_{rr}$)
  - + High output linearity, Low Cross-over Distortion
  - = **Low THD**

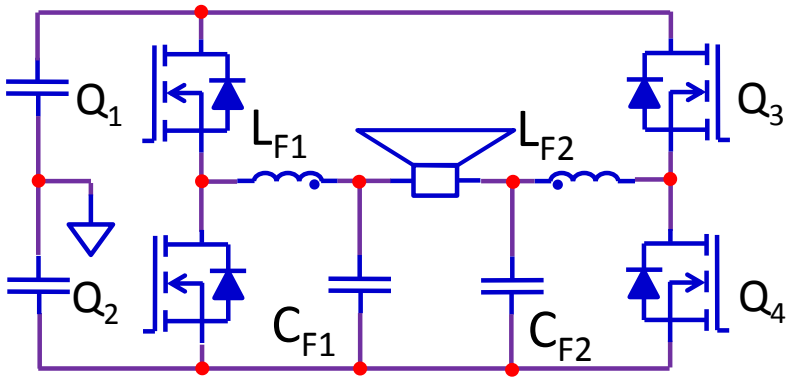


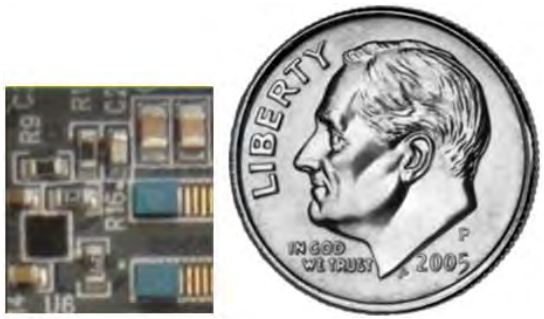



# eGaN FET Class-D Audio Amplifier

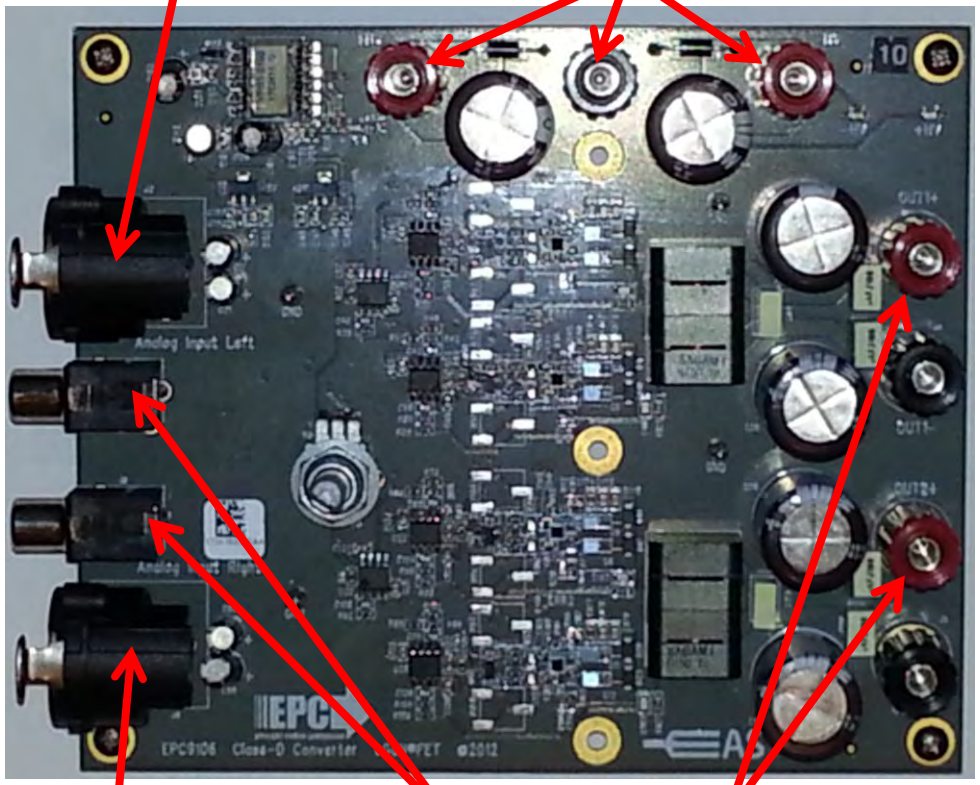


- Bridge-Tied-Load (BTL)
- EPC2016 with LM5113




**eGaN FET Power Stage:**
250 W into 4 Ω at 440 kHz without a heatsink



# A Look Into the Future

# Breaking Down the Barriers



- Does it enable significant new capabilities?
- Is it easy to use?
- Is it VERY cost effective to the user?
- Is it reliable?

# Breaking Down the Barriers



- Does it enable significant new capabilities?
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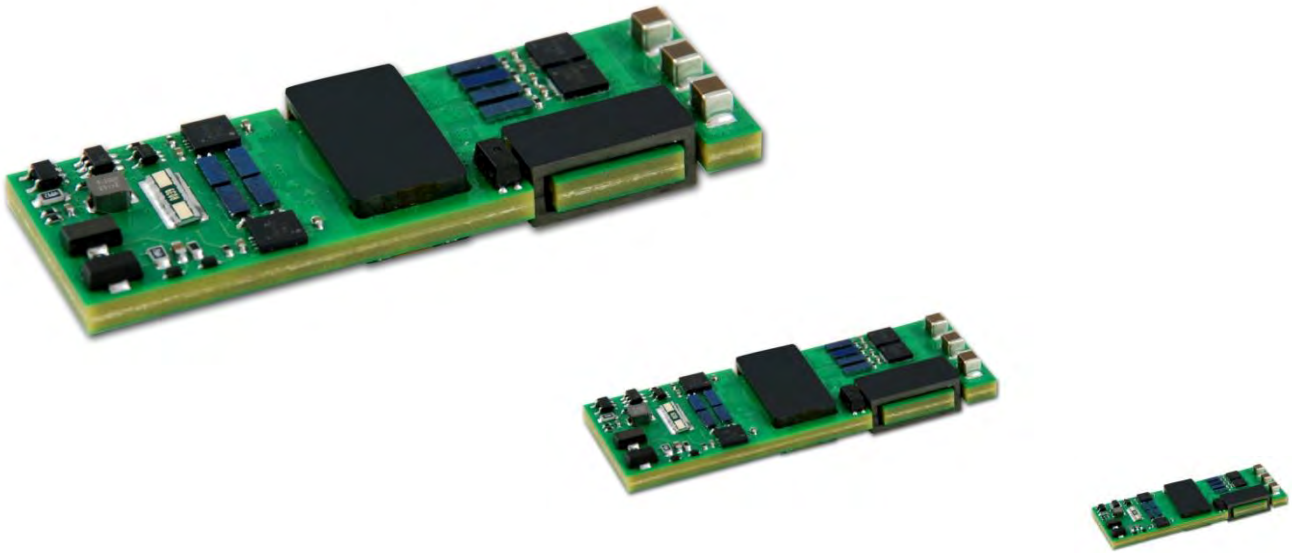
# eGaN FETs are Faster





***Faster Transistors***

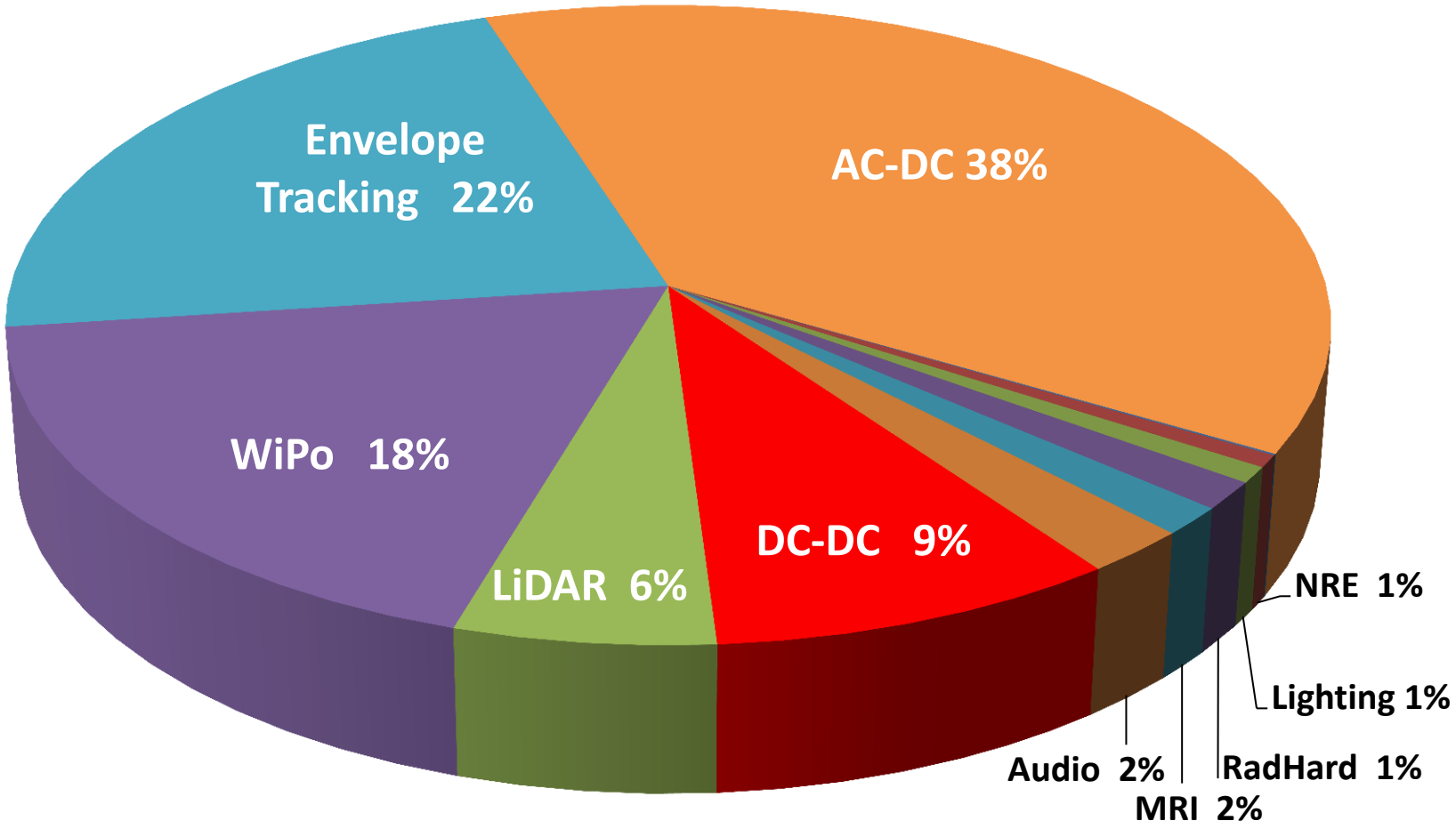
Faster transistors enable the systems to get smaller, more efficient, and lower cost.

# Key Applications



- Wireless Power Transmission
- RF DC-DC "Envelope Tracking"
- LiDAR
- RadHard
- Network and Server Power Supplies
- Point of Load Modules
- Energy Efficient Lighting
- Class D Audio
- Various Medical

# Product Revenue Forecast 2018



# Breaking Down the Barriers



- Does it enable significant new capabilities?
- Is it easy to use?
- Is it VERY cost effective to the user?
- Is it reliable?

# Is an eGaN FET Easy to Use?



**It's just like a MOSFET**

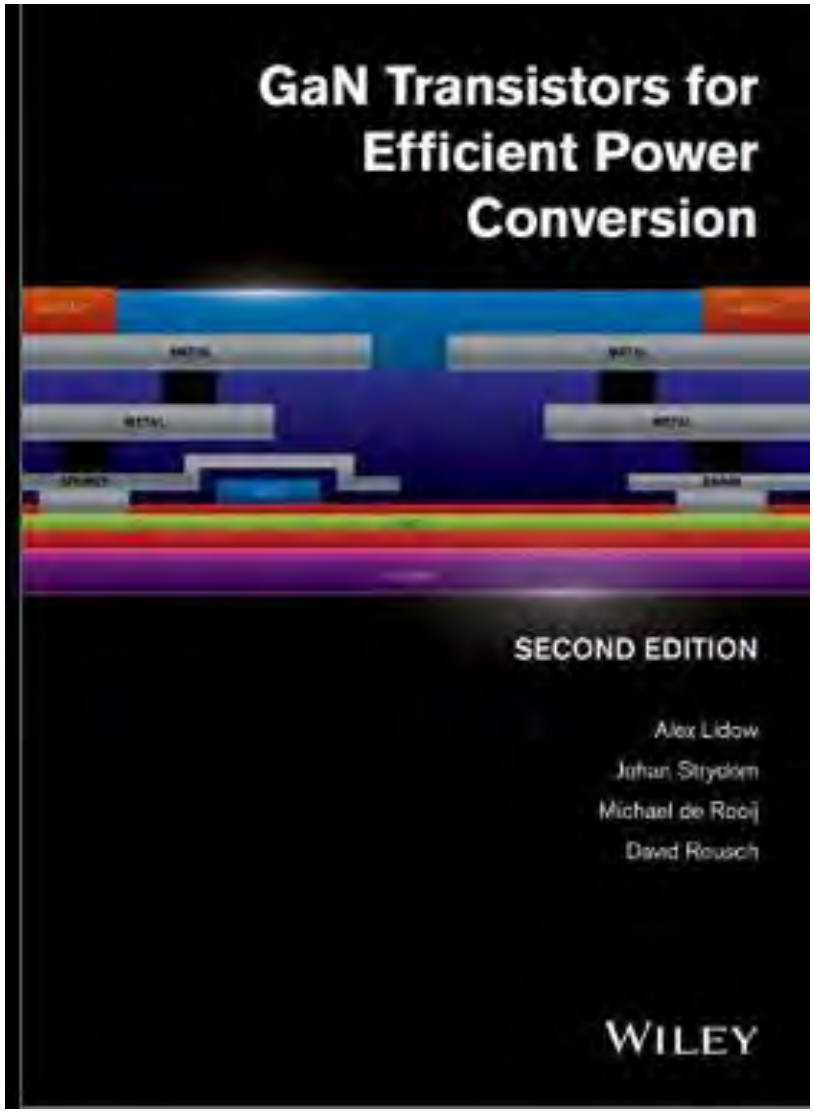
**except**

**The high frequency capability makes circuits using eGaN FETs sensitive to layout**

**The lower $V_{G(MAX)}$ of 6 V makes it advisable to have $V_{GS}$ regulation in your gate drive circuitry**

# Educating




GaN Transistors for Efficient Power Conversion
SECOND EDITION
Alex Lidow
Johan Strydom
Michael de Rooij
David Reusch
WILEY

# Universities with GaN Transistor Programs

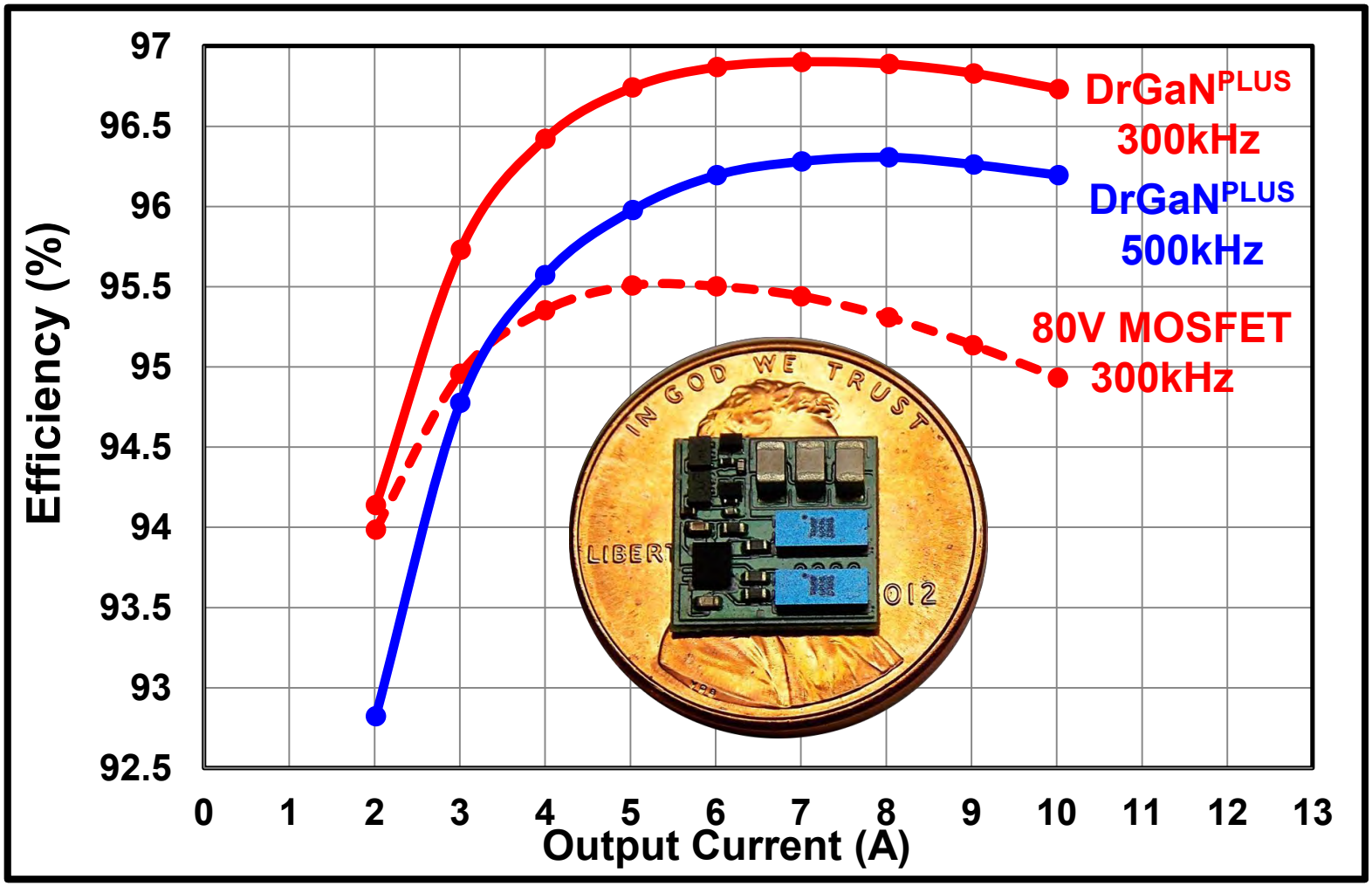


## Universities all over the world are graduating well-trained engineers experienced in the use of GaN Transistors

- Virginia Tech
- University of California at Santa Barbara
- Rensselaer Polytechnic Institute
- Hong Kong University of Science and Technology
- Cornell University
- Katholieke Universiteit Leuven
- University of Bristol
- University of Glasgow
- University of Sheffield
- University of Warsaw
- University of Sydney
- Massachusetts Institute of Technology
- Cambridge University
- National Central University of Taiwan
- National Taiwan University
- Chang Gung University
- University of Florida
- Florida State University
- Case Western University
- Yale University
- University of Ohio, Toledo
- Ohio State University
- Kyushu Institute of Technology
- National Chiao Tung University
- University of Tennessee
- Auburn University
- University of Texas
- Yamaguchi University
- Universitat Kassel
- National Tsinghua University
- Mid Sweden University
- New Mexico State University
- University of Johannesburg
- University of Toronto
- Universita di Padova
- Delft University of Technology
- Missouri University of Science and Technology
- University of Maryland
- Insitituto Italiano di Technologia

# Simplifying GaN- DrGaN$^{PLUS}$






$V_{IN}$=48 V $V_{OUT}$=12 V $f_{sw}$=300 kHz L=10 µH eGaN FET T/SR: 100 V EPC2001
MOSFET T/SR: 80 V BSZ123N08NS3G

# Breaking Down the Barriers



- Does it enable significant new capabilities?
- Is it easy to use?
- Is it VERY cost effective to the user?
- Is it reliable?

# Silicon vs. eGaN Product Costs



| | 2014 | 2015 |
|---|---|---|
| **Starting Material** | lower | lower |
| **Epi Growth** | ***higher*** | ***~same?*** |
| **Wafer Fab** | same | lower |
| **Test** | same | same |
| **Assembly** | lower | lower |
| **OVERALL** | **higher** | ***lower!*** |

# Breaking Down the Barriers



- Does it enable significant new capabilities?
- Is it easy to use?
- Is it VERY cost effective to the user?
- Is it reliable?

# High Temp Reverse Bias (HTRB)

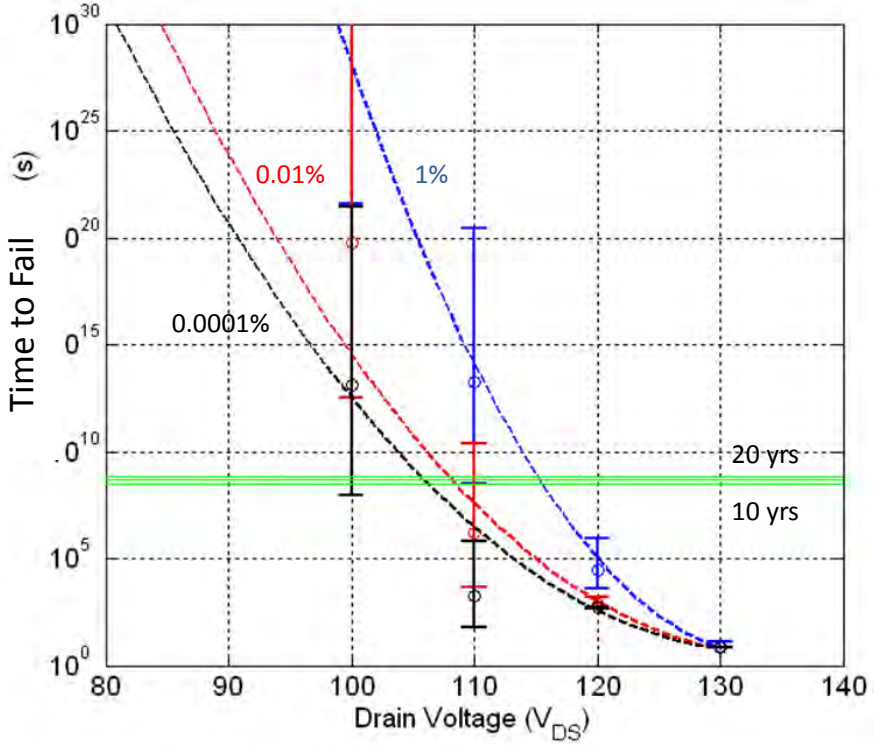


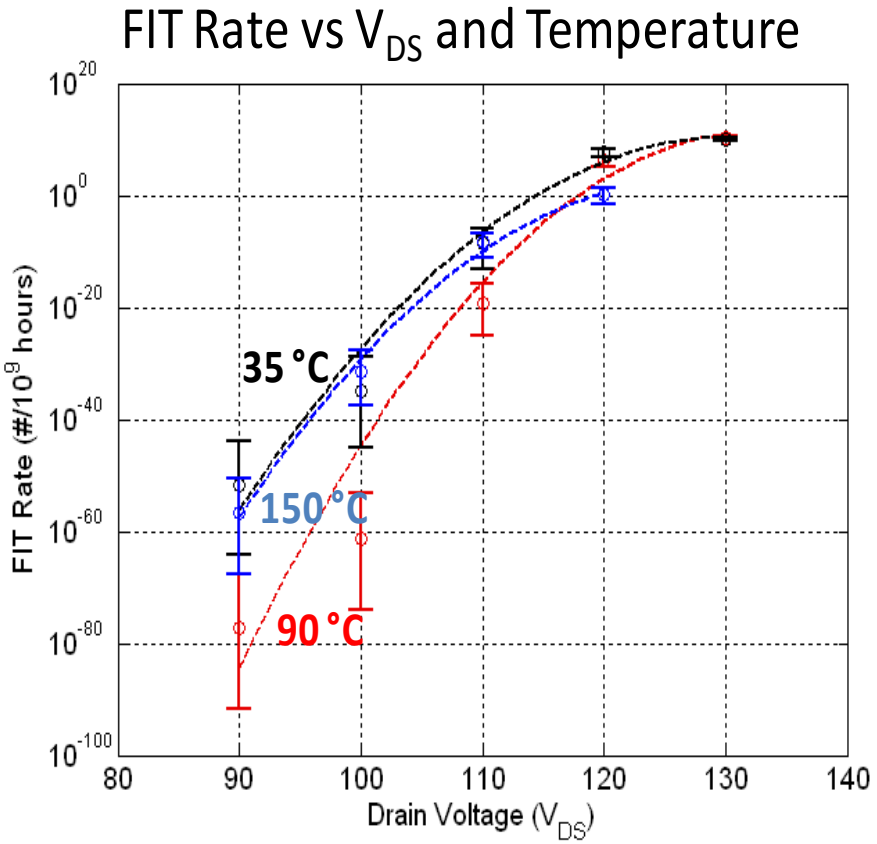
| Part Number | Stress $V_{DS}$ (V) | Temperature (°C) | Sample Size | Results (# of fails) | Duration (Hrs) |
|---|---|---|---|---|---|
| EPC2001 | 80 | 150 | 207 | 0 | 500 |
| EPC2001 | 80 | 150 | 144 | 0 | 168 |
| EPC2001 | 80 | 150 | 80 | 0 | 1000 |
| EPC2001 | 80 | 125 | 96 | 0 | 168 |
| EPC2001 | 100 | 125 | 45 | 0 | 1000 |
| EPC2016 | 80 | 150 | 239 | 0 | 500 |
| EPC2016 | 100 | 150 | 80 | 0 | 168 |

- Over 0.5 million accumulated device hours of reliability testing without failure across 891 devices.

# 100 V HTRB Acceleration

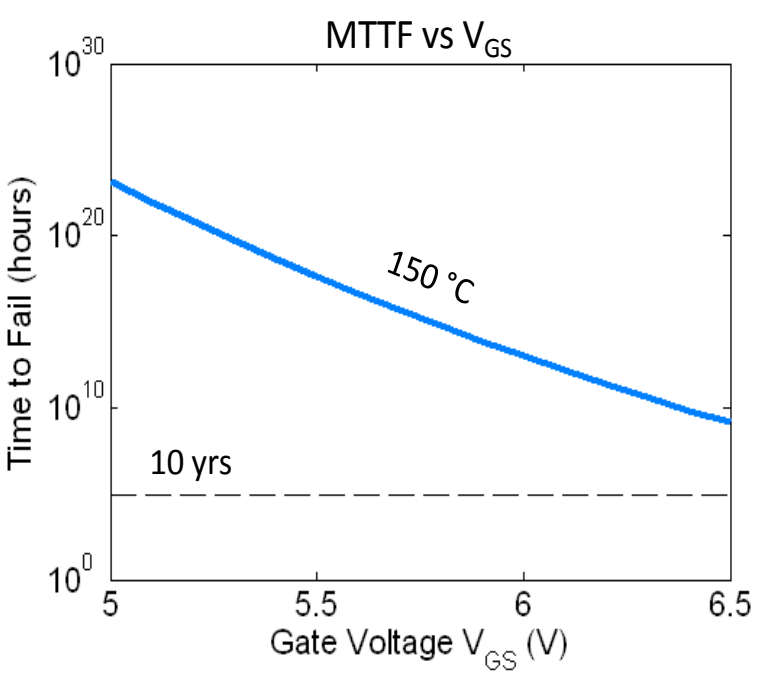


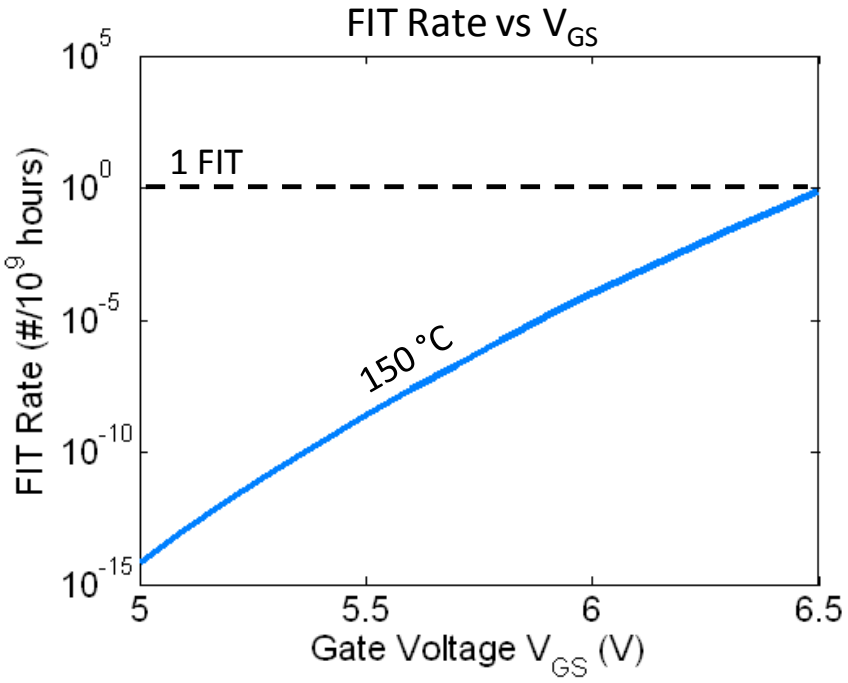


# HTGB Acceleration





# High Temp Gate Bias (HTGB)

| Part Number | Stress $V_{GS}$ (V) | Temperature (°C) | Sample Size | Results (# of fails) | Duration (Hrs) |
|---|---|---|---|---|---|
| EPC2001 | 5 | 150 | 48 | 0 | 168 |
| EPC2001 | 5 | 125 | 167 | 0 | 168 |
| EPC2001 | 5 | 150 | 192 | 0 | 500 |
| EPC2001 | 5 | 150 | 125 | 0 | 1000 |
| EPC2014 | 5 | 150 | 48 | 0 | 500 |
| EPC2015 | 5 | 125 | 96 | 0 | 168 |
| EPC2015 | 5 | 150 | 50 | 0 | 1000 |
| EPC2001 | 5.5 | 150 | 48 | 0 | 168 |
| EPC2001 | 5.5 | 150 | 208 | 0 | 500 |
| EPC2016 | 5.5 | 150 | 80 | 0 | 168 |
| EPC2016 | 5.5 | 150 | 80 | 0 | 500 |
| EPC2001 | 5.75 | 150 | 96 | 0 | 168 |
| EPC2001 | 5.75 | 125 | 32 | 0 | 168 |
| EPC2001 | 5.75 | 125 | 48 | 0 | 181 |
| EPC2001 | 5.75 | 125 | 64 | 0 | 200 |
| EPC2001 | 5.75 | 150 | 240 | 0 | 500 |
| EPC2001 | 5.75 | 125 | 32 | 0 | 500 |
| EPC2016 | 5.75 | 90 | 32 | 0 | 200 |
| EPC2016 | 5.75 | 150 | 32 | 0 | 350 |
| EPC2016 | 5.75 | 150 | 240 | 0 | 500 |
| EPC2019 | 5.75 | 150 | 160 | 0 | 168 |
| EPC2001 | 6 | 125 | 24 | 0 | 181 |
| EPC2001 | 6 | 150 | 32 | 0 | 200 |
| EPC2001 | 6 | 150 | 80 | 0 | 437 |
| EPC2001 | 6 | 150 | 32 | 0 | 500 |
| EPC2001 | 6 | 125 | 32 | 0 | 500 |
| EPC2016 | 6 | 90 | 32 | 0 | 200 |
| EPC2016 | 6 | 150 | 32 | 0 | 350 |
| EPC2001 | 6.3 | 150 | 32 | 0 | 200 |
| EPC2016 | 6.3 | 150 | 32 | 0 | 200 |
| EPC2016 | 6.3 | 90 | 32 | 0 | 200 |
| EPC2016 | 6.6 | 150 | 32 | 0 | 200 |

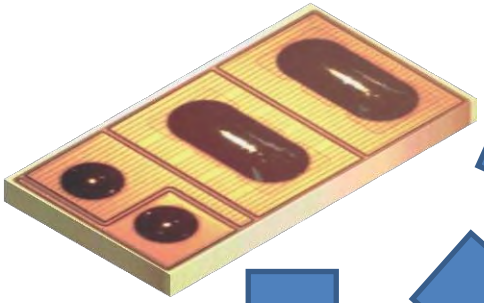
- 0 fail in over 0.97 million accumulated device hours of HTGB reliability testing greater than 5V.
- 0 fail in over 0.6 million accumulated device hours of HTGB reliability testing greater than 5.5V.

# A Look Into the Future

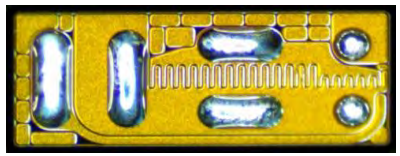
# Moore's Law Revival



Gen 2
2010-2013
40 V - 200 V



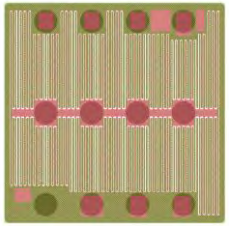
Generation 3
Higher Frequency
Launched September 2013



Generation 4
2 X Performance Improvement
Launched June 2014

Half Bridge ICs
September 2014

High Voltage
September 2014

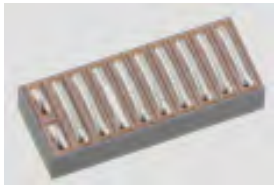


Generation 5
~December 2014

# GaN Integration

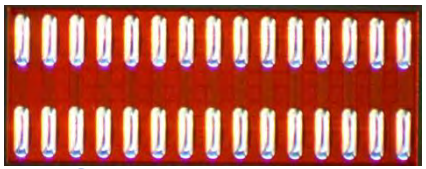


## Generation 2/4 Discrete HB

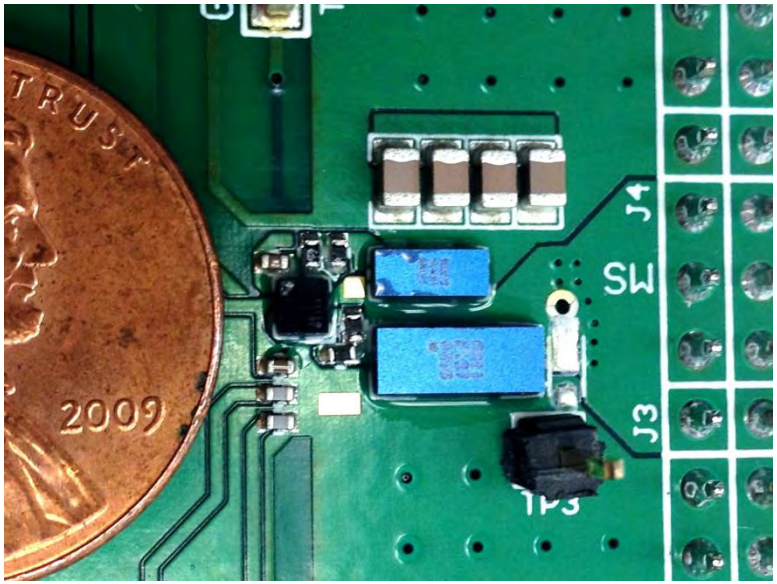


Top Switch (T)

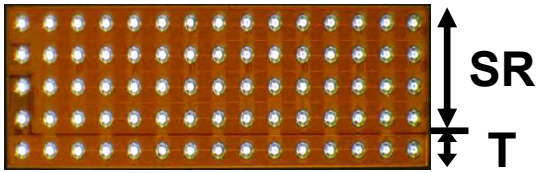
+



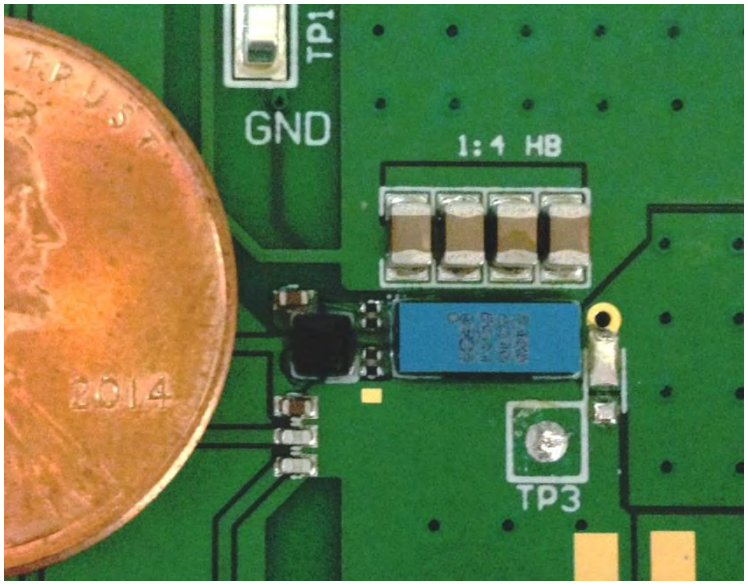
Synchronous Rectifier (SR)




## Generation 4 Monolithic 4:1 HB

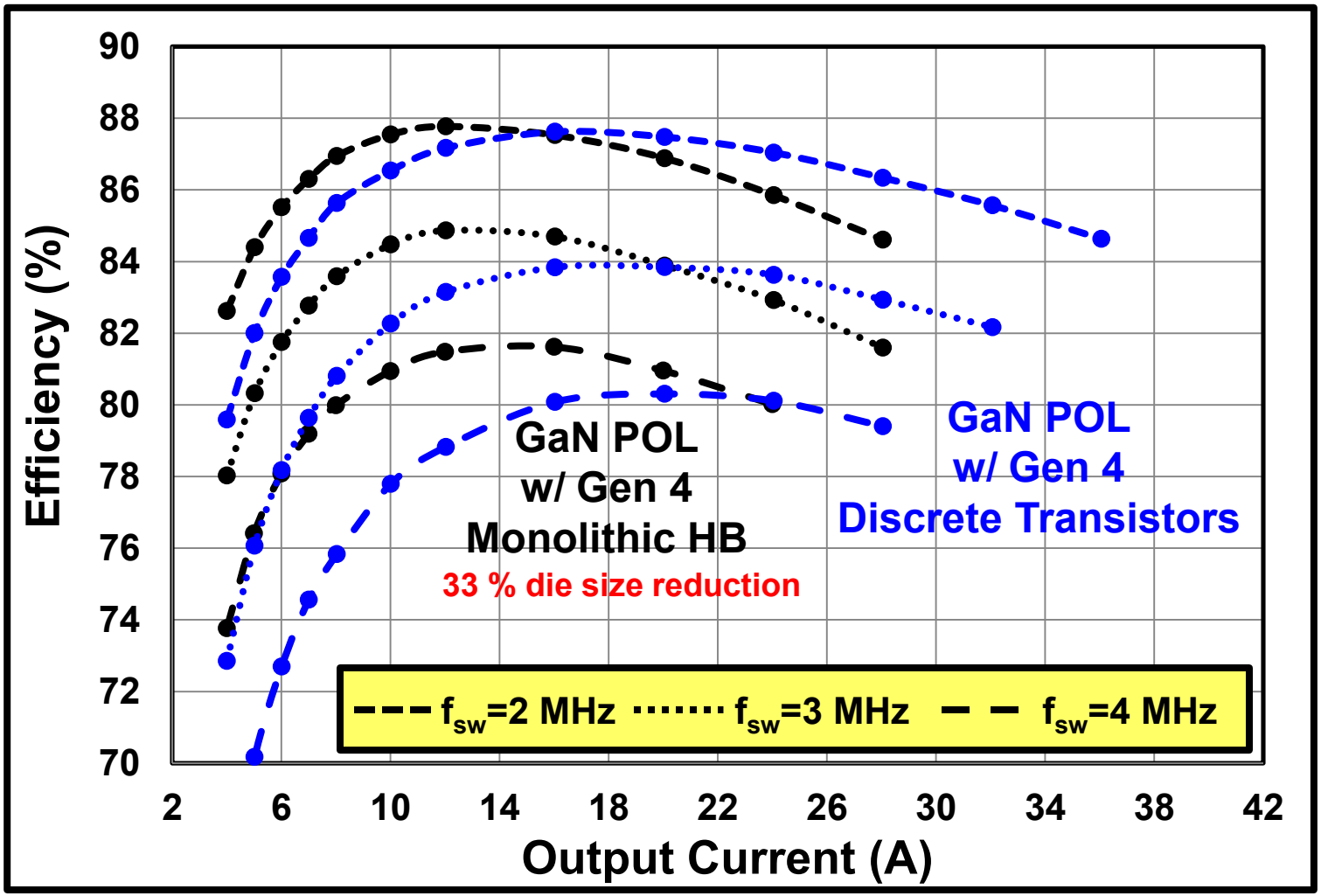



33 % die size reduction



# Monolithic Half Bridge






$V_{IN}$=12 V $V_{OUT}$=1.2 V L=100 nH

# Summary



- GaN transistors enable exciting new applications such as LiDAR, RF Envelope Tracking and Wireless Power Transmission
- GaN transistors have the potential to replace silicon power MOSFETs and LDMOS in power conversion applications with a low-cost and higher efficiency solution
- GaN technology is keeping Moore's Law alive!